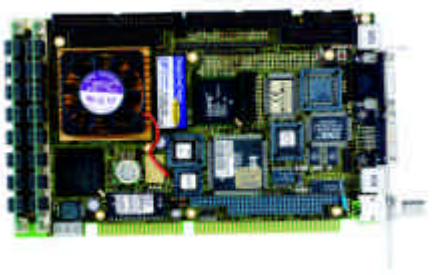
DIGITAL-LOGIC
smart embedded computers

TECHNICAL USER'S MANUAL FOR:

MICROSPACE®

SLOTCARD
PC/104 plus

PCC-P5



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REVISION HISTORY:

Prod.-Serialnumber: From: To:	Product Version	Document Version	Date / by:	Modification: Remarks, News, Attention:
	V1.1	***V1.0***	***01.97 FK***	
		V1.01	01.97 FK	Different Modifications
		V1.1	05.97 FK	HD-PIO Modes
		V1.11	07.97 FK	Corrections
	V2.1a	***V2.1***	***08.97 FK***	***New Board PCC586***
		V2.11	08.97 FK	Modified, Layout
		V2.12	09.97 FK	Modification DLG
		V2.13	03.98 JM	I/O&Memory Map corrected
		V2.14	03.98 JM	Detailed corrections
		V2.15	05.98 JM	Jumper table corrections
		V2.16	06.98 JM	AMIBIOS Setup description included
	V2.2	***V2.20***	***02.99 FK***	***Update, New Board PCC-P5***
		V2.21	02.99 FK	VID4-VID0 Core Voltage added
		V2.22	03.99 JM	Thermoscan pics added
		V2.23	03.99 TS	Related APP-NOTES
		V2.24	09.99 MAJ	V2.2 designs added
		V2.25	11.99 FK	Jumpers mod. , AMD BFx
		V2.26	01.00 STP	Video in pins changed
	V2.3	**V2.27**	**04.2000 STP**	**Jumperlist, connectors added, minor corrections**
	V2.3	V2.3	03.2001 STP	Few updates and corrections

Registration Form:

Please register your product under:

http://www.digitallogic.com -> SUPPORT -> Product Registration

After registration, you will receive driver & software updates, errata information, customer information and news from DIGITAL-LOGIC AG products automatically.

Table of Contents

1 PREFACE

This manual is for integrators and programmers of systems based on the MICROSPACE card family. It contains information on hardware requirements, interconnections, and details of how to program the system. The specifications given in this manual were correct at the time of printing; advances mean that some may have changed in the meantime. If errors are found, please notify DIGITAL-LOGIC AG at the address shown on the title page of this document, and we will correct them as soon as possible.

1.1 Trademarks

MICROSPACE, MicroModule	DIGITAL-LOGIC AG
DOS Vx.y, Windows	Microsoft Inc.
PC-AT, PC-XT	IBM
NetWare	Novell Corporation
Ethernet	Xerox Corporation
DR-DOS, PALMDOS	Digital Research Inc. / Novell Inc.
ROM-DOS	Datalight Inc.

1.2 Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual and specifically disclaims any implied warranty of merchantability or fitness for any particular purpose. DIGITAL-LOGIC AG shall under no circumstances be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage. DIGITAL-LOGIC AG reserves the right to revise this publication from time to time without obligation to notify any person of such revisions. If errors are found, please contact DIGITAL-LOGIC AG at the address listed on the title page of this document.

1.3 Who should use this Product

- Electronic engineers with know-how in PC-technology.
- Without electronic know-how we expect you to have questions. This manual assumes, that you have a general knowledge of PC-electronics.
- Because of the complexity and the variability of PC-technology, we can't give any warranty that the product will work in any particular situation or combination. Our technical support will help you to may get a solution.
- Pay attention to the electrostatic discharges. Use a CMOS protected workplace.
- Power supply OFF when you are working on the board or connecting any cables or devices.

This is a high-technology product.
You need know-how in electronics and PC-technology to install the system !

1.4 Recycling Information

Hardware:

- **Print:** epoxy with glass fiber
  wires are of tin-plated copper
- **Components:** ceramics and alloys of gold, silver
  check your local electronic recycling

Software:

- **no problems:** re-use the diskette after formatting

1.5 Technical Support

1. **Contact your local DIGITAL-LOGIC Technical Support in your country first !**
2. Use the Internet Support Request form at http://www.digitallogic.com -> Support -> Support Request Form
3. Send a FAX or an E-mail to DIGITAL-LOGIC AG with a description of your problem.

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Fax: ++41 32 681 58 01
E-Mail: support@digitallogic.com
Internet www.digitallogic.com

➔ Support requests will only be accepted with detailed information of the product (BIOS-, Board- Version) !

1.6 Limited Warranty

DIGITAL-LOGIC AG warrants the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for one year following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of product and is not transferable.

During the one year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, customers are required to contact the company.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Neither if the user has not enough knowledge of these technologies or has not consulted the product manual or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

Except, as expressly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

2 OVERVIEW

2.1 Standard Features

The MICROSPACE PC is a miniaturized modular device incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

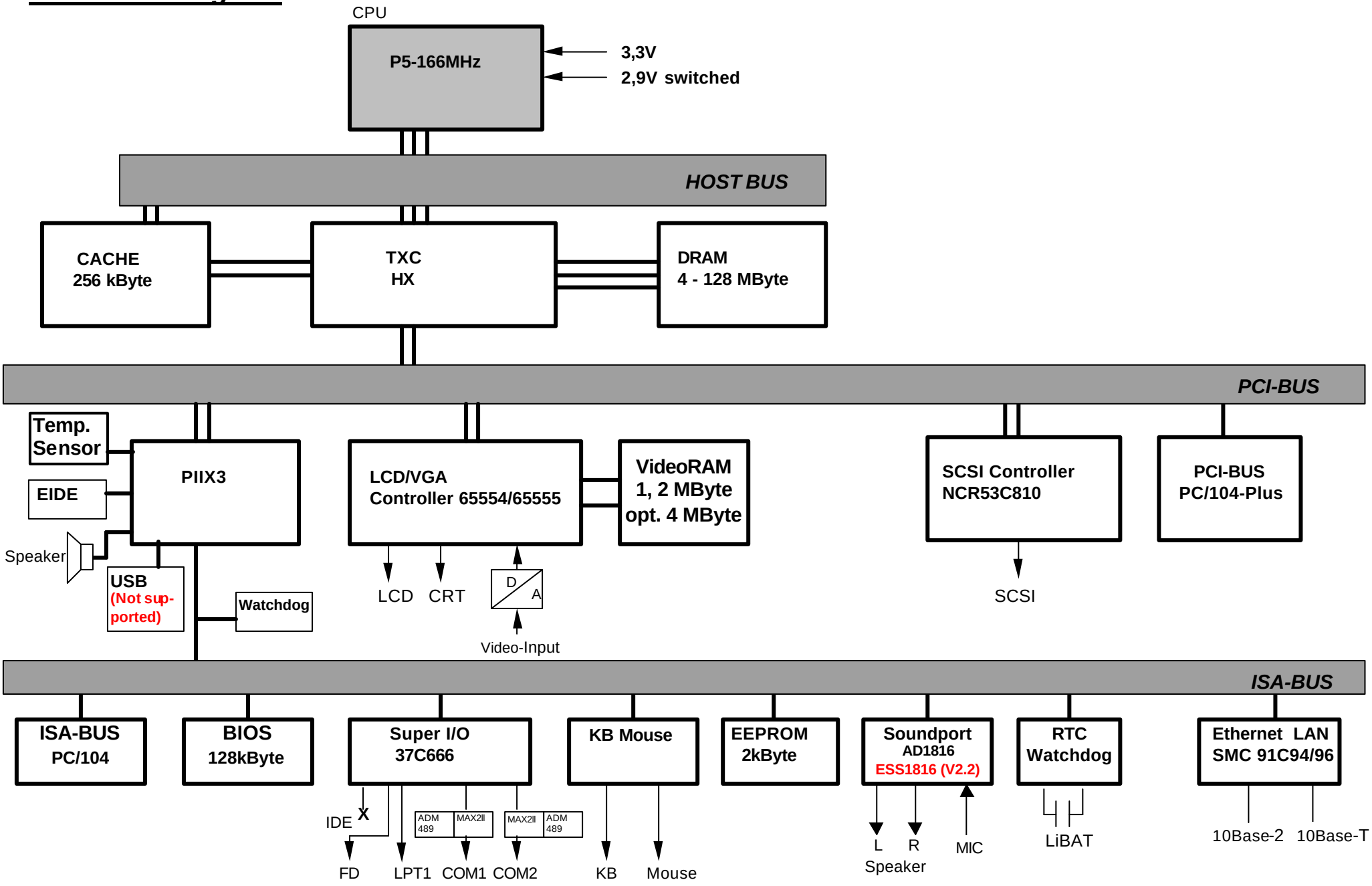
- Powerful PENTIUM CPU 100 MHz up to 200 MHz,
  Supports optional 2.9V CPU's like INTEL-MMX, AMD and CYRIX
- FLASH BIOS , downloadable
- DRAM 4 - 128 MByte
- 256k burst piplined second level cache
- Timers
- DMA
- Real-time clock with CMOS-RAM and battery buffer
- LPT1 parallel port
- COM1, COM2 serial port
- PS/2 keyboard interface
- PS/2 mouse Interface
- SVGA/LC Display interface
- Floppy disk Interface
- E-IDE harddisk interface
- ISA-Bus
- Optional SCSI-2 with 10MB/s
- Optional Ethernet-LAN, 10 Base-2
- Optional Video Input for 3 sources, PAL/NTSC
- Optional Soundport

2.2 Unique Features

The MICROSPACE PCC-P5 includes all standard PC/AT functions plus unique DIGITAL-LOGIC AG enhancements, such as:

- Low-power consumption, 17 watt
- Single 5 volt supply
- Watchdog
- Power-fail circuit
- EEPROM setup and configuration
- Video Input for 3 video sources PAL or NTSC
- DiskOnChip Flashdisk up to 72MByte
- PC/104+ PCI extension
- UL approved parts

2.3 Block Diagram



2.4 PCC-P5 Specifications

CPU:	
CPU 64 Bit:	Pentium 100MHz up to 200MHz
CPU 16 Bit:	None
Mode:	Real / Protected
Compatibility:	8086 – 80486
Word Size:	32 Bits
Physical Addressing:	32 lines
Virtual Addressing:	16 Gbytes
Clock Rates:	100 / 133 / 166 / 200 MHz
Socket Standard:	Socket 7 with 324 pins, 3.3V switched, (Option: 2,9V sw/ 3.3V lin) Since V2.2: free programmable CPU-Voltage 1.6V to 3.5V
2nd. Level Cache:	
available	256k onboard, burst pipelined SRAM for max. performance
PC-Chipset:	
Intel	HX430 (TRITON)
DMA:	
8237A comp.	4 channels 8 Bits 3 channels 16 Bits
Interrupts:	
8259 comp.	8 + 7 levels, PC compatible
Timers:	
8254 comp.	3 programmable counter/timers
Memory:	
DRAM	2 x 72 pin SIMM, 60ns, 4,16, 32, 64, 128MByte
Video Output:	
Controller:	65554 / 65555 from C&T
BUS:	32 Bit highspeed 33 MHz PCI bus
Enhanced BIOS:	Multi VGA / LCD BIOS
Video-Memory:	2 MByte - 32 bit, expandable up to 4MByte
CRT-Monitor:	up to 1600 x 1280 pixels
Flatpanel:	TFT: 640 x 480, 800 x 600, 1024 x 768 STN: 640 x 480 color and monochrome Plasma: up to 1280 x 1024 EL: 640 x 350, 640 x 480
Flatpanelinterface:	Standard: 65554/65555 = TTL
	Optional: 68554 = C&T PanelLink
Controller Modes:	CRT only; Flatpanel only or simultaneous CRT and Flatpanel
Drivers:	Windows 3.11, WIN95, NT3.5, NT4.0 and other applications

Video Input: (option)

Controller:	65554 / 65555 from C&T
BUS:	32 Bit highspeed 33 MHz PCI bus
Videoinput Norm:	3 channels with PAL or NTSC (composite video sources = CVBS) 2 channels YC sources (=SVHS) 2 channels CVBS and 1 channel SVHS V2.1A: may be programmed into the ITT VPX 3220A Since V2.2: Philips SAA7111
Driversupport:	DOS, WIN95 (demosoftware)
Resolution:	320 x 240 with 65554 / 69000 optional: 568 x 720 with 65555 or 69000
Capture speed:	up to 30 images/second
PAL/NTSC Decoder:	until V2.1A ITT VPX 3220A since V2.2: Philips SAA7111A
Y-C resolution:	4:4:4 or 4:2:2 or 4:1:1
RGB resolution:	4:4:4 (16 Bit), gamma corrected

Mass Storage:

FD:	Floppy disk interface, for max. 2 floppies, 34pin connector
HD:	E-IDE interface, 40pin interface up to 12MByte fast IDE transferrates
SCSI Devices:	PCI 10MB/s FAST SCSI-2 up to 7 devices, removable boot media NCR 53C810 PCI SCSI controller

Standard AT interfaces:

Serial:

Name	FIFO	IRQs	Addr.	Standard	Option
COM1	yes	IRQ4	3F8	RS232C	RS422/RS485
COM2	yes	IRQ3	2F8	RS232C	RS422/RS485

(Baudrates: up to 115kBaud), RS485 is an assembling option

Parallel:	LPT1 printer interface, in the EPP Mode bidirectional
Keyboard:	PS/2
Mouse:	PS/2
Speaker:	0.1W output drive
RTC:	146818A compatible RTC with CMOS-RAM 128Byte
Backup current:	< 5µA
Battery:	Lithium 3V (48mAh)

LAN - Ethernet: (option)

Type:	IEEE 802.3
Controller:	SMC 91C94 / 96
Compatibility:	ODI-Novell
Driver:	ODI, packet-driver IEEE 802.3, NT3.5, OS/2, NDIS, NT4.0
Connector:	10Base-T (optionally assembled) 10Base-2 (standard assembled)
Data Rate:	10 MB/sec
Data-Bus:	16 Bit
Cable Type:	RG/58A/U 50 ohms
Remote Boot Socket:	none
RAM Buffer:	4k
Configuration:	with EEPROM

Sound I/O: (option)

Controller:	Until V2.1A: AD1816 8Bit Soundblaster compatible Since V2.2: ESS1869 8Bit Soundblaster compatible, with LM1877
Driver Support:	DOS, WIN 3.11, WIN95, NT4
Output channels:	Stereo Output Line Level
Input:	Microphone, Line
Features:	- Compatible with: SoundBlasterPro 8 Bit, AD-Lib, MicroSoft-Windows Sound System - OPL3 Synthesizer built in - 3D Stereo Enhancement - Digital mixer - Game Port, Midi Interface - Programmable IRQs, DRQs and I/O addresses - Supports 16 Bit type F DMA playback

Supervisory:

Watchdog:	LTC1232 with power-fail detection

USB external:

Controller:	430HX / PIIX3
Transferrate:	12.5MBps / 1.5 MBps

BUS internal:

PCI	IEEE-996 standard bus, by Intel
Clock:	33MHz with 32bit data path and 100MB/s transferrate

BUS external:

ISA	IEEE-996 standard bus
Clock:	8 MHz or programmable

Embedded BUS:

PC/104	IEEE-996 standard bus
Clock:	8 MHz or programmable
PC/104+	PCI 32bit, 33Mhz bus, this is an assembling option

Power Supply:

Working:	5 Volts ± 5%
Current:	3.4A nominal, using P5-166 MHz
Suspend:	2.5A
Rise Time:	>100µs from 0V to 4.75V

Physical Characteristics:

Dimensions:	Length:	200 mm / 7.9"
	Depth:	120 mm / 4,7"
	Height:	50 mm / 1.95"
Weight:	360 gr	
PCB Thickness:	1.6 mm / 0.0625 inches nominal	
PCB Layer:	Multilayer	

Operating Environment:

Relative humidity:	5 - 90% non condensing		
Vibration:	5 to 2000 Hz		
Shock:	10 G		
Temperature:	Operating:	Standard version:	-25°C to +60°C
		Enhanced temp. range:	-25°C to +70°C -E27
	Storage:	-55°C to +85°C	

Cooling:

Standard:	5V Fan, with feedback (frequency sensor)
Temperaturesensor:	onboard, located in the center below the CPU
Option:	passive with air flow > 1000ft/Min.

EMI / EMC (IEC1131-2 refer MIL 461/462):

ESD Electro Static Discharge:	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 metallic protection needed, separate Ground Layer included,15kV single peak
REF Radiated Electromagnetic Field:	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. not tested
EFT Electric Fast Transient (Burst):	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1KV Supply, 500 I/O, 5Khz
SIR Surge Immunity Requirements:	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2 kV, 6 pulse/minute I/O: 500 V, 2 pulse/minute
High-Frequency Radiation:	EN55022

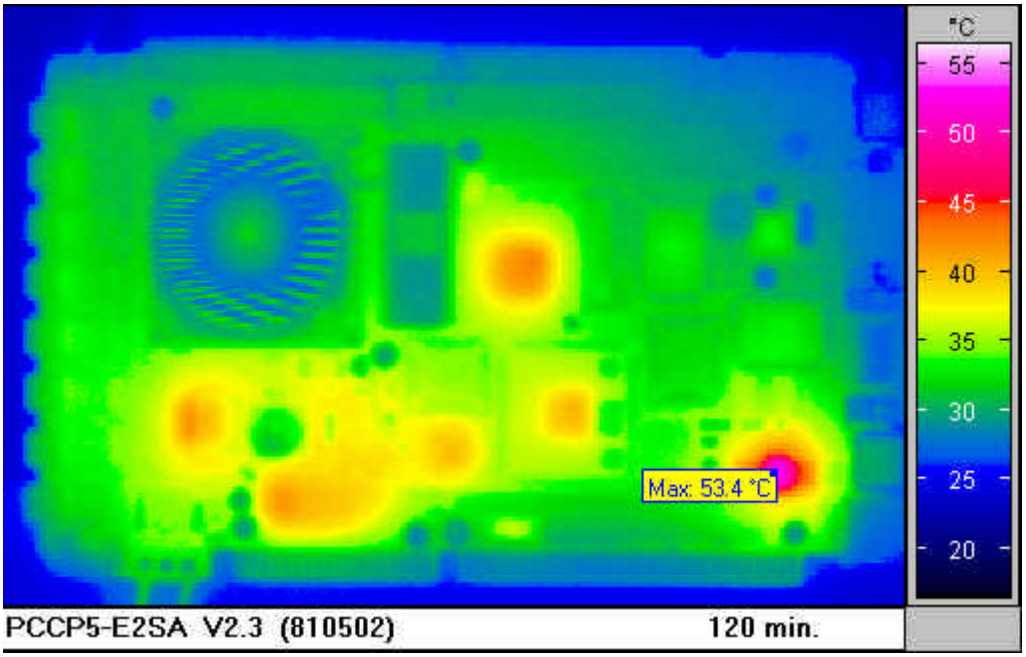
Compatibility:

PCCP5:	mechanically compatible to standard ISA slot cards

Any information is subject to change without notice.

2.5 Thermoscan

Product: PCCP5 Scan time: 120min.



2.6 Ordering Codes

PCCP5	MICROSPACE PCCard without CPU, with 256k Cache no Options
Standard Board:	
PCCP5-E2SA	MICROSPACE PCCard without CPU, with 256k Cache with SCSI, with Sound, with Ethernet
Option - E2	Ethernet LAN 10 Base-2 (BNC)
Option - E1	Ethernet LAN 10 Base-T (twisted pair)
Option - S	SCSI-2
Option - A	Audio Sound Interface
Option -V4M	4MB Video RAM Option
Option P+	PC/104+ PCI Bus
Option -VINP	Video Input 3 channels
Option -R2	RS485 option on the COM2 instead of the RS232C
Option 2.9V/3.3V	OEM production, depending of the used CPU
Option 44pin IDE	OEM production
Option 26pin FDC	OEM production

2.7 BIOS History

Version:	Date:	Status:	Modifications:
V3.20	Aug.98.	released	Y2K tested
V3.21	Nov.98	beta	new version for MSM-P5 V4.0
V3.24	Jun.99	released	Port and setup options

2.8 Related Application Notes

#	Description
64	Bestückungsrichtlinien PCCP5
74	HX-Power Management of DLAG products
77	Ethernet EEPROM values do not match
80	High frequency Radiation (to meet EN55022)
84	Power consumption on Pentium / any other boards with attached drives (HDD, CD)
85	LAN TABLE update MSMP5S

➔ *Application Notes are available at http://www.digitallogic.com ->support, or on any Application CD from DIGITAL-LOGIC.*

2.9 This product is "YEAR 2000 CAPABLE"

This DIGITAL-LOGIC product is "YEAR 2000 CAPABLE". This means, that upon installation, it accurately stores, displays, processes, provides and/or receives date data from, into, and between 1999 and 2000, and the 20. and 21. centuries, including leap year calculations, provided that all other technology used in combination with said product properly exchanges date data with it. DIGITAL-LOGIC makes no representation about individual components within the product should be used independently from the product as a whole. You should understand that DIGITAL-LOGIC's statement that an DIGITAL-LOGIC product is "YEAR 2000 CAPABLE" means only that DIGITAL-LOGIC has verified that the product as a whole meet this definition when tested as a stand-alone product in a test lab, but dies not mean that DIGITAL-LOGIC has verified that the product is "YEAR 2000 CAPABLE" as used in your particular situation or configuration. DIGITAL-LOGIC makes no representation about individual components, including software, within the product should they be used independently from the product as a whole.

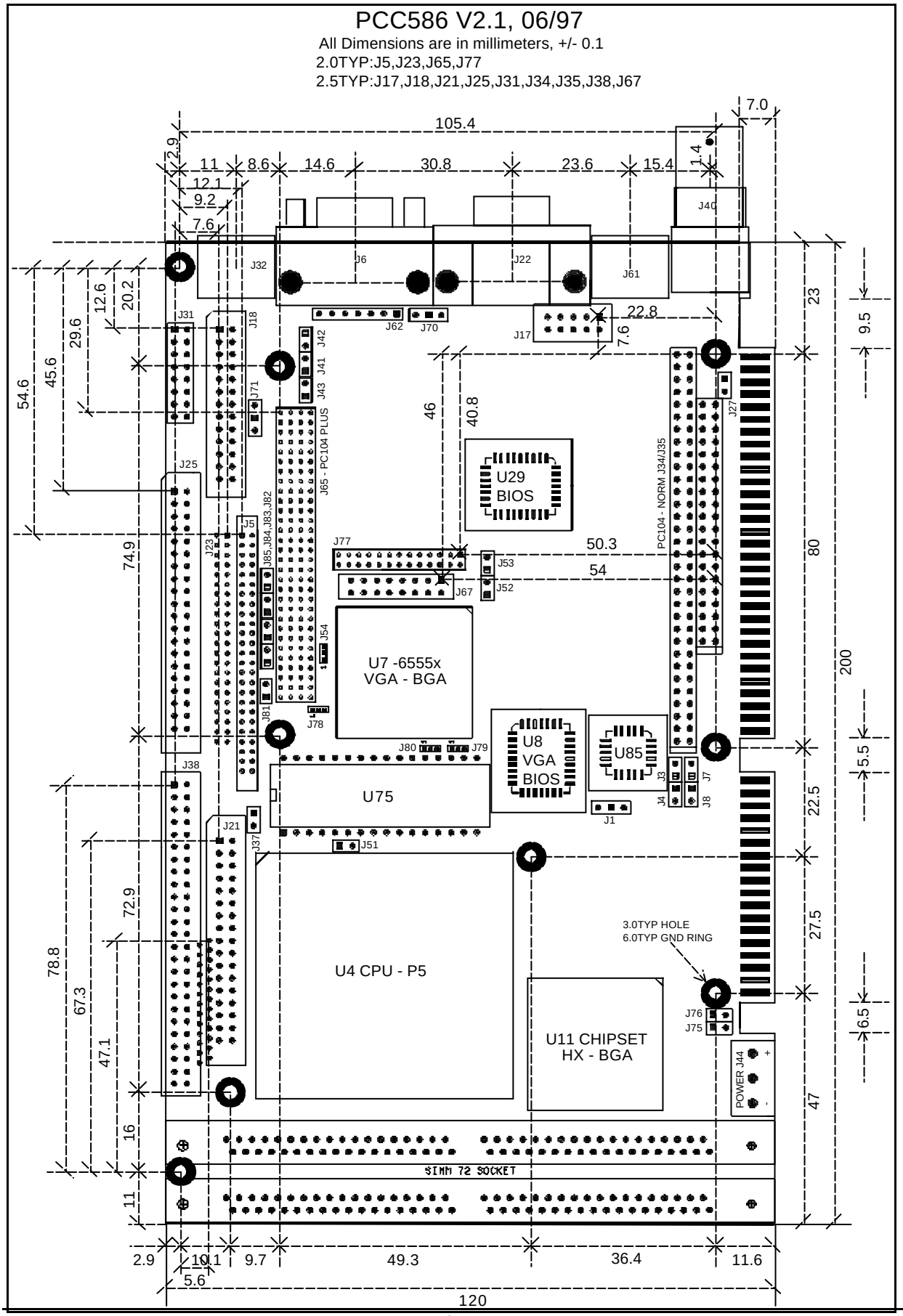
DIGITAL-LOGIC customers use DIGITAL-LOGIC products in countless different configurations and in conjunction with many other components ans systems, and DIGITAL-LOGIC has no way to test wheter all those configurations and systems will properly handle the transition to the year 2000. DIGITAL-LOGIC encourages its customers and others to test whether their own computer systems and products will properly handle the transition to the year 2000.

The only proper method of accessing the date in systems is indirectly from the Real-Time-Clock via the BIOS. The BIOS in DIGITAL-LOGIC computerboards contain a century checking and maintenance feature the checks the laest two significant digits of the year stored in the RTC during each BIOS request (INT 1A) to read the date and, if less than '80' (i.e. 1980 is the first year supported by the PC), updates the century byte to '20'. This feature enables operating systems and applications using BIOS date/time services to reliably manipulate the year as a four-digit value.

2.10 PCC-P5L Incompatibilities to a standard PC/AT

No incompatibilities are observed.

2.11 Mechanical Dimensions



3 THE ISA AND PC/104 BUS SIGNALS

AEN, output
Address Enable is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. **low = CPU Cycle , high = DMA Cycle**

BALE, output
Address Latch Enable is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. This signal is used so that devices on the bus can latch LA17..23. The SA0..19 address lines latched internally according to this signal. BALE is forced high during DMA cycles.

/DACK[0..3, 5..7], output
DMA Acknowledge 0 to 3 and 5 to 7 are used to acknowledge DMA requests (DRQO through DRQ7). They are **active low**. This signal indicates that DMA operation can begin.

DRQ[0..3, 5..7], input
DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK/) line goes active. DRQO through DRQ3 will perform 8-bit DMA transfers; DRQ5-7 are used for 16 accesses.

/IOCHCK, input
IOCHCK/ provides the system board with parity (error) information about memory or devices on the I/O channel. **low = parity error , high = normal operation**

IOCHRDY, input
I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lengthen I/O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of one clock cycle (67 nanoseconds). This signal should be held low for no more than 2.5 microseconds. **low = wait, high = normal operation**

/IOCS16, input
I/O 16 bit Chip Select signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/0 cycle. It is derived from an address decode. /IOCS16 is **active low** and should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 20mA. The signal is driven based only on SA15-SAO (not /IOR or /IOW) when AEN is not asserted. In the 8 bit I/O transfer, the default transfers a 4 wait-state cycle.

/IOR, input/output
I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is **active low**.

/IOW, input/output
I/O Write instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is **active low**.

IRQ[3 - 7, 9 - 12, 14, 15], input
These signals are used to tell the microprocessor that an I/O device needs attention. An interrupt request is generated when an IRQ line is **raised from low to high**. The line must be held high until the microprocessor acknowledges the interrupt request .

/Master, input
This signal is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/0 channel may issue a DRQ to a DMA channel in cascade mode and receive a /DACK.

/MEMCS16, input
MEMCS16 Chip Select signals the system board if the present data transfer is a 1 wait-state, 16-bit, memory cycle. It must be derived from the decode of LA17 through LA23. /MEMCS16 should be driven with an open collector (300 ohm pull-up) or tri-state driver capable of sinking 2OmA.

/MEMR input/output
These signals instruct the memory devices to drive data onto the data bus. /MEMR is active on all memory read cycles. /MEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /MEMR, it must have the address lines valid on the bus for one system clock period before driving /MEMR active. These signals are **active low**.

/MEMW, input/output
These signals instruct the memory devices to store the data present on the data bus. /MEMW is active in all memory read cycles. /MEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /MEMW, it must have the address lines valid on the bus for one system clock period before driving /MEMW active. Both signals are **active low.**

OSC, output
Oscillator (OSC) is a high-speed clock with a 70 nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle. OSC starts 100us after reset is inactive.

RESETDRV, output
Reset Drive is used to reset or initiate system logic at power-up time or during a low line-voltage outage. This signal is active high. When the signal is active all adapters should turn off or tri-state all drivers connected to the I/O channel. This signal is driven by the permanent Master.

/REFRESH, input/output
These signals are used to indicate a refresh cycle and can be driven by a microprocessor on the I/0 channel. These signals are **active low**.

SAO-SA19, LA17 - LA23 input/output
Address bits 0 through 19 are used to address memory and I/0 devices within the system. These 20 address lines, allow access of up to 1MBytes of memory. SAO through SA19 are gated on the system bus when BALE is high and are latched on the falling edge of BALE. LA17 to LA23 are not latched and addresses the full 16 MBytes range. These signals are generated by the microprocessors or DMA controllers. They may also be driven by other microprocessor or DMA controllers that reside on the I/0 channel. The SA17-SA23 are always LA17-LA23 address timings for use with the MSCS16 signal. This is advanced AT96 design. The timing is selectable with jumpers LAxx or SAxx.

/SBHE, input/output
Bus High Enable (system) indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. Sixteen-bit devices use /SBHE to condition data-bus buffers tied to SD8 through SD15.

SD[O..15], input/output
These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/0 devices. DO is the least-significant bit and D15 is the most significant bit. All 8-bit devices on the I/O channel should use DO through D7 for communications to the microprocessor. The 16-bit devices will use DO through D15. To support 8-bit device, the data on D8 through D15 will be gated to DO through D7 during 8-bit transfers to these devices; 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

/SMEMR input/output
These signals instruct the memory devices to drive data onto the data bus for the first MByte. /SMEMR is active on all memory read cycles. /SMEMR may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/0 channel wishes to drive /SMEMR, it must have the address lines valid on the bus for one system clock period before driving /SMEMR active. The signal is **active low**.

/SMEMW, input/output
These signals instruct the memory devices to store the data present on the data bus for the first MByte. /SMEMW is active in all memory read cycles. /SMEMW may be driven by any microprocessor or DMA controller in the system. When a microprocessor on the I/O channel wishes to drive /SMEMW, it must have the address lines valid on the bus for one system clock period before driving /SMEMW active. Both signals are **active low.**

SYSCLK, output
This is a 8 MHz system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

TC output
Terminal Count provides a pulse when the terminal count for any DMA channel is reached. The TC completes a DMA-Transfer. This signal is expected by the onboard floppy disk controller.

/OWS, input
The Zero Wait State (/OWS) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, /OWS is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of one-wait states, /OWS should be driven active one system clock after the Read or Write command is active, gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. /OWS is **active low** and should be driven with an open collector or tri-state driver capable of sinking 2OmA.

12V +/- 5%
used only for the flatpanel backligth supply only.

GROUND = 0 Volt
used for the entire system.

VCC, +5V +/- 0.25 Volt
3-4 Amp. nominal, peak current of HD, SCSI-Devices and Cache could go up to 8 Amp..

3.1 Expansion Bus

The bus currents are:

Output-Signals:	IOH:	IOL:
D0 - D16	24mA	24mA
A0 - A23:	24mA	24mA
MR,MW,IOR,IOW, RES,ALE,AEN,C14	24mA	24mA
DACKx, DRQx,INTx, PSx, OPW	24mA	24mA

Input-Signals:	Logic-Family:	Voltage:
	ABT-Logic	ABT-Logic
Input Signals:	ViH(min.) = 2.15V	ViL(max.) = 0.85V

4 DETAILED SYSTEM DESCRIPTION

This system has a system configuration based on the ISA architecture. Check the I/O and the Memory map in this chapter.

4.1 Power Requirements

The power is connected through the ISA Bus connector, or the PC/104 Power connector, or the separate power connector on the board. The supply uses only +5V and ground connection. For backplane supply and the Flash BIOS operation, the user has to connect the 12V (only for LCD port).

Warning: Make sure that the power plug is wired correctly before supplying power to the board! A built-in diode protects the board against reverse polarity.

Tolerance of 5 V supply: 5Volt ± 5%; Power-fail signal starts at ± 10% of 5 volt nominal and generates a reset status for the MICROSPACE PC.

ATTENTION: With the harddisk connected to the IDE 44pin interface, the power requirement is high. The peak current must be enough to spin up the HD-motor. The typical spin-up current of the harddisk is 0.8 - 1.5Amp at 5V. Too little current will drop the voltage under 5 volts for a short time. Due to this undervoltage, the system or the harddisk stops or falters. The VGA could also be "snowy".

The precise power requirements of the MICROSPACE PCC-P5 depends on a number of factors, including what functions are present on the board and what peripherals are connected to the board's I/0 ports. For example, AT-keyboards draw their power from the keyboard connector on the MICRO-SPACE PCC-P5 board, and therefore add keyboard current to the total power drawn by the board from its power supply.

CPU:	Clock:	Memory:	no Harddisk	HD-500MByte:	HD-PowerUp:
P5-133	133MHz	32 MByte	3.5 A	4.0 A	5 A
Suspended		32 Mbyte	1.6 A		
HD start current:		ST-9096A Seagate 2,5" 80 MBytes		ca. 0.8 Amp.	
AT-keyboard:				ca. 10 mA	

4.2 CPUs, Boards and RAMs

4.2.1 CPUs of this MICROSPACE Product

Proposed:	Standard:	INTEL P5 from 100MHz to 200MHz	(single 3.3V switched)
	Option:	INTEL MMX P5	(dual voltage , switched 2.9V , linear 3.3V I/O)
	Option:	AMD K6	(dual voltage , switched 2.9V , linear 3.3V I/O)
	Option:	Cyrix M2	(dual voltage , switched 3.1V , linear 3.3V I/O)

The CPU type must be defined by ordering. The switched mode voltage regulator must be tuned to the correct core voltage of the CPU and the linear 3.3V regulator may be assembled.

4.3 Interfaces

4.3.1 PS/2-Keyboard

Standard PS2-Keyboard , also available on the utilityconnector

4.3.2 PS/2-Mouse Interface

Standard PS/2 conector , also available on the utilityconnector

4.3.3 Line Printer Port LPT1

A standard bi-directional LPT port is integrated into the MICROSPACE PC, with DMA7 support.

Further information about these signals is available in numerous publications, including the IBM technical reference manuals for the PC and AT computers and from some other reference documents.

The current is: IOH = 12mA IOL = 24mA

The SMC 37C665 may be programmed in the BIOS Setup.

Since V2.2: The A10 is connected to the SMC37C665. Therefore the EPP/ECP modes are available.

4.3.4 Serial Ports COM1-COM2

The serial channels are fully compatible with 16C550 UARTS. COM1 is the primary serial port, and is supported by the board's ROM-BIOS as the PC-DOS 'COM1' device. The secondary serial port is COM2; it is supported as the 'COM2' device.

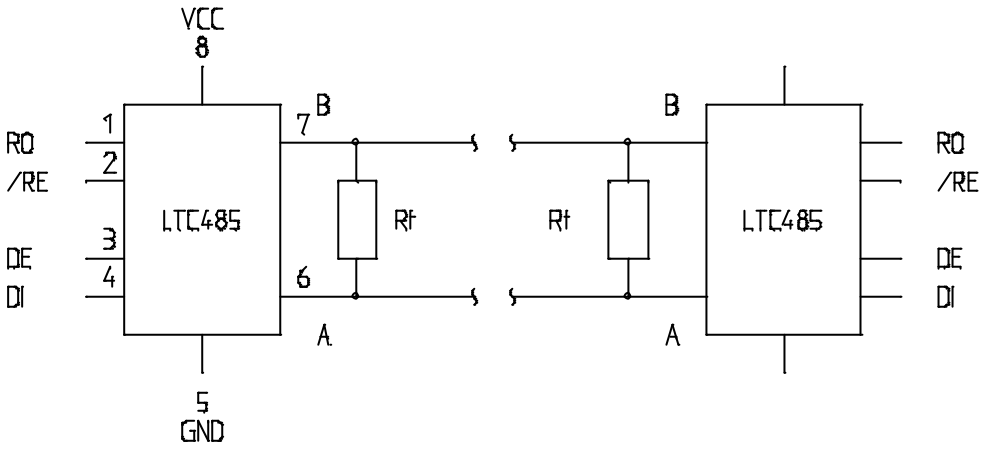
Standard: COM 1/2: 16C550: 2 x 16C550 with 16 Byte FIFO

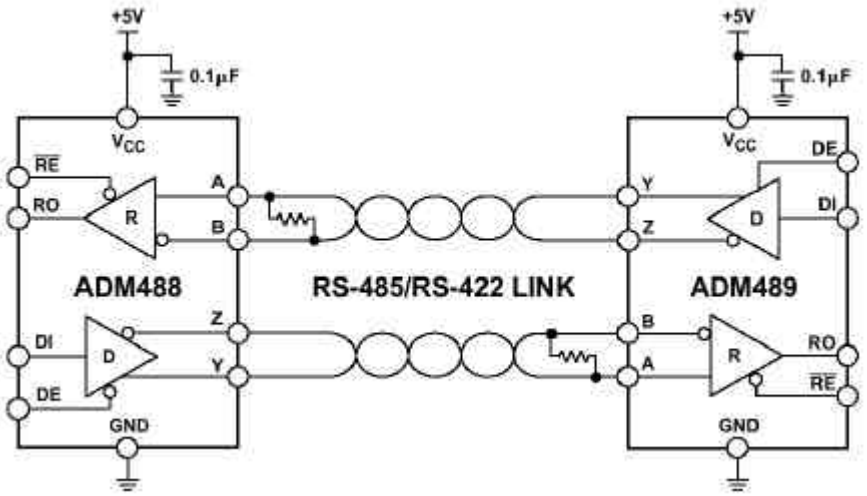
Serial Port Connectors - COM1, 2 generally

Pin	Signal Name	Function	in/out	DB25 Pin	DB9 Pin
1	CD	Data Carrier Detect	in	8	1
2	DSR	Data Set Ready	in	6	6
3	RXD	Receive Data	in	3	2
4	RTS	Request To Send	out	4	7
5	TXD	Transmit Data	out	2	3
6	CTS	Clear to Send	in	5	8
7	DTR	Data Terminal Ready	out	20	4
8	RI	Ring Indicator	in	22	9
9	GND	Signal Ground		7	5

The serial port signals are compatible with the RS232C specifications.

- Until boardversion V2.1, the RS422/485 (2wire) was an assembling option instead of the RS232
- Since boardversionV2.2, connector J91 and J93 are RS422/485 (4wire) ports





4.3.5 Floppy disk interface

The onboard floppy disk controller and ROM-BIOS support one or two floppy disk drives in any of the standard PC-DOS and MS-DOS formats shown in the table . 2.88MB floppy are not supported.

4.3.5.1 Supported floppy formats

Capacity	Drive size	Tracks	Data rate	DOS version
1.2 MB	5-1/4"	80	500 KHz	3.0 - 6.22
720 K	3-1/2"	80	250 KHz	3.2 - 6.22
1.44 M	3-1/2"	80	500 KHz	3.3 - 6.22

4.3.5.2 Floppy interface connector

We support only CMOS drives. That means that the termination resistors are 1 kOhm. 5 1/4“-drives are not recommended (TTL interface).

The 34 pin Connector: Ribbon 1,27mm IDT dual row terminal with 2.54mm grid
The 26 pin Connector: Optional: FFC/FPC 0.3mm thick 1.0mm (0.039") pitch (MOLEX 52030 Serie) on the rear side mounted

Floppy Disk Interface Connector

FD34: Pin	FD26: Pin	Signal Name	Function	in/out
2	---	-RPM/-RWC	Speed/Precomp (option)	out
4	---	(Not used)		
6	---	(Not used)		
8	2	-IDX	Index Pulse	in
10	---	-MO1	Motor On 1	out
12	4	-DS2	Drive Select 2	out
14	---	-DS1	Drive Select 1	out
16	10	-M02	Motor On 2	out
18	12	-DIRC	Direction Select	out
20	14	-STEP	Step	out
22	16	-WD	Write Data	out
24	18	-WE	Write Enable	out
26	20	-TRKO	Track 0	in
28	22	-WP	Write Protect	in
30	24	-RDD	Read Data	in
32	26	-HS	Head Select	out
34	6	-DCHG	Disk Change	in
1-33	25,23,21,19,17	GND	Signal grounds	
	1,3,5	VCC	+5 Volt	

4.3.6 Speaker interface

One of the board's CPU device provides the logic for a PC compatible speaker port. The speaker logic signal is buffered by a transistor amplifier, and provides approximately 0.1 watt of audio power to an external 8 ohm speaker. The speaker must be connected to VCC (and not to Ground).

We propose to use a serial capacitor of 1µF with the speaker to eliminate any DC-current to protect the speaker itself from overheating.

4.4 Controllers

4.4.1 Interrupt Controllers

An 8259A compatible interrupt controller, within the chipset device, provides seven prioritized interrupt levels. Of these, several are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt	Sources	onboard used
IRQ0	ROM-BIOS clock tick function, from timer 0	yes
IRQ1	Keyboard controller output buffer full	yes
IRQ2	Used for cascade 2. 8259	yes
IRQ3	COM2	yes
IRQ4	COM1	yes
IRQ5	Free for user	no
IRQ6	Floppy controller	yes
IRQ7	LPT1 parallel printer	yes
IRQ8	Battery backed clock, alarm function of the RTC	yes
IRQ9	Free for user	no
IRQ10	Ethernet (LAN), standard selection	yes
IRQ11	Free for user	no
IRQ12	PS/2 mouse	yes
IRQ13	Math coprocessor	yes
IRQ14	Harddisk IDE / SCSI	yes
IRQ15	Free for user	no

4.5 Timers and Counters

4.5.1 Programmable Timers

An 8253 compatible timer/counter device is also included in the board's ASIC device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190 MHz clock, derived from a 14.318 MHz oscillator, which can be internally divided down to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

Timer Assignment

Timer	Function
0	ROM-BIOS clock tick (18.2 Hz)
1	DRAM refresh request timing (15 µS)
2	Speaker tone generation time base

4.5.2 Battery backed clock (RTC)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with that in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

One unique feature of the board's battery-backed clock device is that it contains the backup battery directly on the board. The battery is rated for a minimum of 6 years of clock and internal CMOS RAM backup under conditions of no power to the board. The battery is removable for easy exchange with a new type or replacement when the battery is exhausted.

The battery is Digital-Logic replacement part: PCC-P5 3V-BAT. The battery-backed clock can be set by using the DIGITAL-LOGIC AG SETUP at boot-time.

Addresses:	70h	=	Index register
	71h	=	Data transfer register
RTC-Address MAP:	00 - 0F		RTC (Real time clock)
	10 - 3F		BIOS setup (Standard)
	40 - 7F		Extended BIOS or SuperState BIOS setup

The chipset consumes the following currents:

Typical battery current at 25°C : <5 µA

4.5.3 Watchdog

The watchdog timer detects a system crash and performs a hardware reset. After powering-up, the watchdog is always disabled as the BIOS does not send strobes to the watchdog. In case the user wants to take advantage of the watchdog, the application must produce a strobe at least every 800 ms. If no strobe occures within the 800 ms, the watchdog resets the system.

To program the watchdog in user applications DIGITAL-LOGIC AG has implemented a special BIOS extension in Interrupt 60h (function: EBh).

Calling this function by setting a 1 in the AL- Register, turns on the watchdog and performs a strobe. Calling the same function with a 0 in the AL-Register, turns off the watchdog.

The following part has to be implemented in the users application:

Watchdog on: The application has to call interrupt 15h function EBh and set a 1 into the AL-register at least every 800 ms.

Watchdog off: The application has to call interrupt 15h function EBh and set a 0 into the AL-register within 800 ms after the last strobe has been sent while the watchdog was still in function (if the watchdog is not turned off in time, it will reset the system again!).

See also chapter 9.4.1

4.6 BIOS

4.6.1 ROM-BIOS Sockets

An EPROM socket with 8 Bit wide data access normally contains the board's AT compatible ROM-BIOS. The socket takes any of a 27C010 to 29F010 EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this socket. The ROM-BIOS sockets occupies the memory area from C0000H through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so this area is already usable for ROM-DOS and BIOS expansion modules. Consult the appropriate address map for the MICROSPACE PCC-P5 ROM-BIOS sockets.

4.6.1.1 Standard BIOS FLASH 29F010

DEVICE:	29F010 PLCC32	with 90ns access time
MAP:	E0000 - FFFFFh	Chipset BIOS from AMI including the SCSI BIOS

4.6.1.2 VGA BIOS FLASH 29F010

DEVICE:	29F010 PLCC32	with 90ns access time (with 29F020 are 4 BIOS Segments with 64k jumper selectable)
Segment-MAP:	C0000 - CBFFF	VGA BIOS 32k or 44k

4.6.2 EEPROM Memory for Setup

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery is running down, the checksum error would appear and stop the system. The capacity of the EEPROM is 2048 Bytes.

Organisation of the 2048Byte EEPROMs:

Address MAP:	Function:
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Keymatrix-Setup valid (01=valid)**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial-Number**
0110h-0113h	Production date (year/day/month)
0114h-0117h	1. Service date (year/day/month)
0118h-011Bh	2. Service date (year/day/month)
011Ch-011Fh	3. Service date (year/day/month)
0120h-0122h	Booterrors (Autoincremented if any booterror occurs)
0123h-0125h	Setup Entries (Autoincremented on every Setup entry)
0126h-0128h	Low Battery (Autoincremented everytime the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Autoincremented on every poweron start)
0130h	Number of 512k SRAM
0131h	Number of 512k Flash
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE (‘M’=PC/104, ‘E’=Euro, ‘W’=MSWS, ‘S’=Slot, ‘C’=Custom)
0137h	CPU TYPE (01h=ELAN300/310, 02h=ELAN400, 03h=486SLC, 04h=486DX, 05h=P5).
0200h-03FFh	**Keymatrix-Setup data**
0200h-027Fh	Keymatrix Table
0400h-07FFh	**Free for Customer’s use**

4.6.3 CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64 bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128 bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain System BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of Day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of Day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A Bit 7 = Update in progress Bits 6-4 = Time based frequency divider Bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B Bit 7 = Run/Halt 0 Run 1 Halt Bit 6 = Periodic Timer 0 Disable 1 Enable Bit 5 = Alarm Interrupt 0 Disable 1 Enable Bit 4 = Update Ended Interrupt 0 Disable 1 Enable Bit 3 = Square Wave Interrupt 0 Disable 1 Enable Bit 2 = Calendar Format 0 BCD 1 Binary Bit 1 = Time Format 0 12-Hour 1 24-Hour Bit 0 = Daylight Savings Time 0 Disable 1 Enable
0Ch	Status Register C Bit 7 = Interrupt Flag Bit 6 = Periodic Interrupt Flag Bit 5 = Alarm Interrupt Flag Bit 4 = Update Interrupt Flag Bits 3-0 = Reserved
0Dh	Status Register D Bit 7 = Real Time Clock 0 Lost Power 1 Power

Continued...

CMOS Map Continued...

Location	Description
0Eh	CMOS Location for Bad CMOS and Checksum Flags bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad
0Fh	Shutdown Code
10h	Diskette Drives bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 K 0010 = Drive A = 1.2 MB 0011 = Drive A = 720 K 0100 = Drive A = 1.44 MB 0101 = Drive A = 2.88 MB bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 K 0010 = Drive B = 1.2 MB 0011 = Drive B = 720 K 0100 = Drive B = 1.44 MB 0101 = Drive B = 2.88 MB
11h	Reserved
12h	Fixed (Hard) Drives bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 Types 1 - 14 1111 = Extended drive types 16-44. See location 19h. bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 Types 1 - 14 1111 = Extended drive types 16-44. See location 2Ah. See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
13h	Reserved

Continued...

CMOS Map Continued...

Location	Description
14h	Equipment bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome bits 3-2 = Reserved bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed
15h	Base Memory Size (in KB) - Low Byte
16h	Base Memory Size (in KB) - High Byte
17h	Extended Memory Size in (KB) - Low Byte
18h	Extended Memory Size (in KB) - High Byte
19h	Extended Drive Type - Hard Drive 0 See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
1Ah	Extended Drive Type - Hard Drive 1 See the *Fixed Drive Type Parameters Table* in Chapter 2 for information on drive types 16-44.
1Bh	Custom and Fixed (Hard) Drive Flags bits 7-6 = Reserved bit 5 = Internal Floppy Diskette Controller 0 = Disabled 1 = Enabled bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled bit 3 = Hard Drive 0 Custom Flag 0 = Disable 1 = Enabled bit 2 = Hard Drive 0 IDE Flag 0 = Disable 1 = Enabled bit 1 = Hard Drive 1 Custom Flag 0 = Disable 1 = Enabled bit 0 = Hard Drive 1 IDE Flag 0 = Disable 1 = Enabled

Continued...

CMOS Map Continued...

Location	Description
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 bytes (48 bits) contain the following data: Cylinders 10 bits range 0-1023 Landing Zone 10 bits range 0-1023 Write Precomp 10 bits range 0-1023 Heads 8 bits range 0-15 Sectors/Track 8 bits range 0-254
1Fh	Byte 0 bits 7-0 = Lower 8 Bits of Cylinders
20h	Byte 1 bits 7-2 = Lower 6 Bits of Landing Zone bits 1-0 = Upper 2 Bits of Cylinders
21h	Byte 2 bits 7-4 = Lower 4 Bits of Write Precompensation bits 3-0 = Upper 4 Bits of Landing Zone
22h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 Bits of Write Precompensation
23h	Byte 4 bits 7-0 = Number of Heads
24h	Byte 5 bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 bytes (48 bits) contain the following data: Cylinders 10 bits range 0-1023 Landing Zone 10 bits range 0-1023 Write Precomp 10 bits range 0-1023 Heads 8 bits range 0-15 Sectors/Track 8 bits range 0-254
25h	Byte 0 bits 7-0 = Lower 8 Bits of Cylinders
26h	Byte 1 bits 7-2 = Lower 6 Bits of Landing Zone bits 1-0 = Upper 2 Bits of Cylinders
27h	Byte 2 bits 7-4 = Lower 4 Bits of Write Precompensation bits 3-0 = Upper 4 Bits of Landing Zone

Continued...

CMOS Map Continued...

Location	Description
28h	Byte 3 bits 7-6 = Reserved bits 5-0 = Upper 6 Bits of Write Precompensation
29h	Byte 4 bits 7-0 = Number of Heads
2Ah	Byte 5 bits 7-0 = Sectors Per Track
2Bh	Boot Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Ch	SCU Password bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password bits 6-0 = Calculated Password
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (KB) detected by POST - Low Byte
31h	Extended RAM (KB) detected by POST - High Byte
32h	BCD Value for Century
33h	Base Memory Installed bit 7 = Flag for Memory Size 0 = 640KB 1 = 512KB bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage bits 7-6 = Reserved bit 5 = Semaphore for Completed POST bit 4 = Semaphore for 0 Volt POST (not currently used) bit 3 = Semaphore for already in SCU menu bit 2 = Semaphore for already in PM menu bit 1 = Semaphore for SCU menu call pending bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

4.6.4 BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the default values will be loaded after resetting the RTC/CMOS-RAM with the CMOS-RESET jumper. If the battery is down, it is always possible to start the system with the default values from the BIOS.

The following entries may be made:

Date:	The current Real Date of the RTC	
Time:	The current Real Time of the RTC	
Drive A or B:	none	= no drive present, FLASHDisk enabled (if device is loaded)
	360k	= 5,25" low density drive or FLASHDISK
	1,2 MB	= 5,25" high density drive or SRAMDISK
	720 K	= 3,5" low density drive
	1,44 MB	= 3,5" high density drive (Default for A:)
	The A: Drive is the bootable drive.	
Display type:	CRT:	for Mono CRT's but no LCD operating possible.
	40 x 25:	for Color CGA or LCD
	80 x 25:	for Color CGA or LCD (Default)
	VGA:	for VGA
Harddisk type:	defines which drive is connected Type = 0 means no drive is present (Default)! Drive Type 48 and 49 let you define a custom harddisk parameter. PRESS the AUTODETECT FUNCTION to identify the HD!	

WARNING:

On the next Setup pages (switched with PgDn and PgUp) the values for special parameters are modifiable. Normally the parameters are set correctly by DIGITAL-LOGIC AG. Be very careful in modifying any parameter since the system could crash. Some parameters are dependent on the CPU type. The cache parameter is always available, for example. So, if you select too few wait states, the **system will not start** until you reset the CMOS-RAM using the **RTC-Reset jumper**, but the default values are reloaded. If you are not familiar with these parameters, do not change anything.

4.6.5 CMOS Setup Harddisk list

Harddisk parameter selection

Since the BIOS autodetects the harddisk type, no HD-drive parameter table is used.
Go into the BIOS-HD-Setup and press autodetect. The parameters are read out of the IDE harddisk and stored in the CMOS memory.

4.6.6 Harddisk PIO Modes

Block Mode (Multi-Sector) Transfer: Block mode boots IDE drive performance by increasing the amount of data transferred.

No Block Mode: 512 Byte per interrupt
Block Mode: up to 64 kByte per interrupt

LBA Mode: LBA (logical block addressing) is a new method of addressing data on a disk drive. In the standard ST506 (MFM) ISA hard disk, data is accessed via a cylinder - head - sector format.

LBA Mode disabled: max. 528 Mbyte per Disk

LBA Mode enabled: max. 8 Gbyte per Disk

Attention:
The BIOS enables the LBA Mode only, if the harddisk was formatted on a system with enabled LBA. If the drive (capacity > 528MB) is formated on a system with disabled LBA, the AMI BIOS will never enable the LBA mode !

The maximum parameters are:
1024 Cyl. , 16 heads, 63 Sec/Track

32 Bit Transfer: Some operating system can handle two 16bit word as one 32bit access. This accelerates the IDE transfer.

Advanced PIO Modes:

PIO-Mode:		Timing:	Transferspeed:	Remarks:	
IDE	0		600ns	2 Mbyte/sec	Slowest I/O
IDE	1		383ns	5.5Mbyte/sec	Standard I/O
EIDE	2		240ns	8.3Mbyte/sec	Fast I/O, Mem.
EIDE	3		180ns	11,3Mbyte/sec	IORDY Protocol
EIDE	4		120ns	16,6Mbyte/sec	IORDY Protocol
EIDE	DMA 1		160ns	13,3Mbyte/sec	DRQ, ATA-2

Begin always with the PIO-Mode 0
in the manual mode (not autodetect) to test a new drive or if you becomes trouble in the automatic mode.
The autodetect mode selects with some drives wrong PIO modes.

4.6.7 EEPROM saved CMOS setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing system informations like: version, production date, customisation of the board, CPU type.
- Storing user/application values.

The EEPROM will be updated automatically after exiting the BIOS setup menu. The system will operate also without any CMOS battery. While booting up, the CMOS is automatically updated with the EEPROM values.

Press the Esc-key while powering on the system before the video shows the BIOS message and the CMOS will **not** be updated.

This would be helpful, if wrong parameters are stored in the EEPROM and the setup of the BIOS does not start.

If the system hangs or a problem appears, the following steps must be performed:

1. Reset the CMOS-Setup (use the jumper to reset or disconnect the battery for at least 10 minutes).
2. Press Esc until the system starts up.
3. Enter the BIOS Setup: a) load DEFAULT values
   b) enter the settings for the environment
   c) exit the setup
4. Restart the system.

- The user may access the EEPROM through the INT15 special functions. Refer to the chapter 9.4.1.
- The system information are read onyl information. To read, use the SFI functions.

4.7 Download the VGA-BIOS and the CORE-BIOS

Before downloading a BIOS, please check as follows:

- Select the SHADOW option in the BIOS, for a BIOS and VGA (if this option is available).
- Disable the EMM386 or other memory managers in the CONFIG.SYS of your bootdisk.
- Make sure, that the DOWN_xxx.EXE programm and the BIOS to download are on the same path and directory!
- Boot the DOS without config.sys & autoexec.bat -> press “F5” while starting DOS boot.
- Is the empty diskspace, where the down.exe is located, larger than 64kB (for safe storage)
- Is the floppydisk not write-protected

Start the DOWNLOADING Tool with:

- Start the corresponding download tool. Refer to the table to see which tool fits in, each productgroup has its own download tool. Do never use the wrong one!

Product:	BIOS-Core download	VGA-BIOS download	BIOS-Ext. download
File-Extension:	*.COR	*.V40 , *.V45 *.V48 depending on the product	*.BIN
BIOS Size:	128k	32k	32k
Addressrange:	E0000 - FFFFFh	C0000 – C7FFFh	C8000 - CFFFFh
MSM386SN	DOWN_3SN.EXE	-	-
MSM386SV	DOWN_3SV.EXE	DOWN_3SV.EXE	DOWN_3SV.EXE
MSM486SL	DOWN_4SN.EXE	-	-
MSM486SN	DOWN_4SN.EXE	-	-
MSM486SV	DOWN_4SV.EXE	DOWN_4SV.EXE	DOWN_4SV.EXE
MSM486SE / SEV	DOWN_4SE.EXE	DOWN_4SE.EXE	-
MSM486DN	DOWN_4DX.EXE	-	-
MSM486DX	DOWN_4DX.EXE	DOWN_4DX.EXE	DOWN_4DX.EXE
SM-486PC / EK	DOWN_SM4.EXE	On the –EK : DOWN_SM4.EXE	-
SM-486PCX / EK	DOWN_S4X.EXE	DOWN_S4X.EXE	DOWN_S4X.EXE
MSM5x86DX	DOWN_4DX.EXE	DOWN_4DX.EXE	DOWN_4DX.EXE
MSM586SEN / SEV	To be defined	To be defined	
MSM-P5	- AMI82602.EXE or - FLASHAMI.COM (AMIBOOT.ROM)**	DOWN_000.EXE	-
PCC-P5L / PCC-PII AMI- BIOS	AMI82602.EXE	DOWN_000.EXE	-
PCC-P5L / PCC-PII PCC-P5S / PCC-P3S PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	-
MSM-P5S MSM-P5SV / SEV AMI- BIOS	AMI82602.EXE	DOWN_000.EXE	-
MSM-P5SN / SEN AMI- BIOS	AMI82602.EXE	-	-
MSM-P5S MSM-P5SV / SEV PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	-
MSM-P5SN / SEN PHOENIX- BIOS	PHLASH.EXE PLATFORM.BIN	-	-
MSEBX	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	
SMP5PC / 3PC / DK	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	
MAS-P5 / P3	PHLASH.EXE PLATFORM.BIN	DOWN_000.EXE	

Remarks:
** Core- file has to be renamed as written in brackets

4.7.1 VGA- BIOS Download Function

The BIOS for the VGA must be downloaded, before a LCD is connected. This could be also a new LCD- display, which needs a corresponding VGA- BIOS.

How to download a VGA- BIOS:

1. Restart the system with the SHADOW enabled (if available) and no EMM386 loaded.
2. Check, if you find the DOWN_xxx.EXE and the *.V40 / *.000 files on your disk, to get downloaded.
3. Refer to the VGABIOS.DOC for more information about the VGABIOS files.
4. Insert the floppydisk with the program DOWN_xxx.EXE and all VGA-Drivers.
5. Start DOWN_xxx.EXE.
6. Check, if the DOWN program has identified the product and the shadow correctly.
7. Select the function PROGRAMM VGA- BIOS.
8. Select the VGA- BIOS out of the proposed file list (UP/DOWN arrows) and press ENTER.
9. Check, if the new VGA- header is displayed on the VGA- INFO- screen.
10. After proceeding, switch off the power and restart the board (cold start).

If the download does not work:
- Check, if no EMM386 is loaded.
- Check, if no peripheral card is in the system, which occupies the same memory range. Disconnect this card.
- If the download is stopped or not completed, make only a warm boot and repeat the steps or download another file. As the video is may shadowed, everything is visible and a cold boot would clear the screen and nothing would be visible afterwards.

If the screen flickers or is misaligned after reboot:
- The previously loaded VGA- BIOS is not corresponding 100% or works only on the LCD properly.

If the screen is dark after the reboot of the system:
- A new system BIOS must be programmed. Ask DIGITAL-LOGIC AG for the binary file.

If the previous version is still programmed:
- Switch off the board and do not make a warm boot due to the fact that the data may are still stored in the memory shadow.

4.8 Memory

4.8.1 Onboard DRAM Memory

Speed: 60ns
Size: 2 x 72pins SIMM
Bits: 36 Bit
Capacity: 8 MBytes, 16 MBytes, 32 MBytes, 64 MBytes
Bank: allways two banks must be equipped

Size combinations:	Bank1	Number of Big SIMMs	Total	Interleaved
	1MBx36	2	8 MBytes	
	2MBx36	2	16 MBytes	
	4MBx36	2	32 MBytes	
	8MBx36	2	64 MBytes	

4.8.2 System Memory Map

The CPU used as a central processing unit on the MICROSPACE PC has a memory address space which is defined by 32 address bits. Therefore, it can address 1GByte of memory. The memory address MAP is as follows:

CPU P5

Address	Size	Function / Comments
000000 - 09FFFFh	640 KBytes	Onboard DRAM for DOS applications
0A0000 - 0BFFFFh	128 KBytes	CGA, EGA, LCD Video RAM 128kB
0C0000 - 0CFFFFh	64 KBytes	Reserved for expansion bus ROMs: C000 - CC00 for VGA BIOS
0D0000 - 0DFFFFh	64 KBytes	Free or DiskOnChip DOC2000 Module from MSystems
0E0000 - 0EFFFFh	64 KBytes	PCI-System BIOS incl. SCSI-BIOS
0F0000 - 0FFFFFh	64 KBytes	PCI-System BIOS incl. SCSI-BIOS
100000 - 1FFFFFh	1 MByte	DRAM for extended onboard memory
200000 - FFFFFFh	14 MBytes	DRAM for extended onboard memory

Attention: Only the D-Segment is free for the user, to use EMM386 or HIMEM programs
If the DOC2000 module is used, the D-Segment is also used, and no EMM386 may be used. For the HIMEM use the EMM386 with the option NOEMS !

Urgent: The AMI POWER BIOS for the P5 has a size of 128k and this value is definitiv, that means may be not decreased !

4.8.3 System I/O Map

The following table shows the detailed listing of the I/O port assignments used in the MICROSPACE board:

I/O Address	Read/Write Status	Description
0000h	R / W	DMA channel 0 address byte 0 (low), then byte 1
0001h	R / W	DMA channel 0 word count byte 0 (low), then byte 1
0002h	R / W	DMA channel 1 address byte 0 (low), then byte 1
0003h	R / W	DMA channel 1 word count byte 0 (low), then byte 1
0004h	R / W	DMA channel 2 address byte 0 (low), then byte 1
0005h	R / W	DMA channel 2 word count byte 0 (low), then byte 1
0006h	R / W	DMA channel 3 address byte 0 (low), then byte 1
0007h	R / W	DMA channel 3 word count byte 0 (low), then byte 1
0008h	R	DMA channel 0-3 status register bit 7 = 1 Channel 3 request bit 6 = 1 Channel 2 request bit 5 = 1 Channel 1 request bit 4 = 1 Channel 0 request bit 3 = 1 Terminal count on channel 3 bit 2 = 1 Terminal count on channel 2 bit 1 = 1 Terminal count on channel 1 bit 0 = 1 Terminal count on channel 0

Continued...

I/O Address	Read/Write Status	Description
0008h	W	DMA channel 0-3 command register bit 7 = DACK sense active high/low 0 low 1 high bit 6 = DREQ sense active high/low 0 low 1 high bit 5 = Write selection 0 Late write selection 1 Extended write selection bit 4 = Priority 0 Fixed 1 Rotating bit 3 = Timing 0 Normal 1 Rotating bit 2 = Controller enable/disable 0 Enable 1 Disable bit 1 = Memory-to-memory enable/disable 0 Disable 1 Enable bit 0 = Reserved
0009h	W	DMA write request register
000Ah	R / W	DMA channel 0-3 mask register bits 7-3 = Reserved bit 2 = 0 Clear bit 1 Set bit bits 1-0 = Channel Select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3
00Bh	W	DMA channel 0-3 mode register bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 0 01 Channel 1 10 Channel 2 11 Channel 3

Continued...

I/O Address	Read/Write Status	Description
000Ch	W	DMA clear byte pointer flip/flop
000Dh	R	DMA read temporary register
000Dh	W	DMA master clear
000Eh	W	DMA clear mask register
000Fh	W	DMA write mask register
0020h	W	Programmable Interrupt Controller - Initialization Command Word 1 (ICW1) provided bit 4 = 1 bits 7-5 = 000 Used only in 8080 or 8085 mode bit 4 = 1 ICW1 is used bit 3 = 0 Edge triggered mode 1 Level triggered mode bit 2 = 0 Successive interrupt vectors separated by 8 bytes 1 Successive interrupt vectors separated by 4 bytes bit 1 = 0 Cascade mode 1 Single mode bit 0 = 0 ICW4 not needed 1 ICW4 needed
0021h	W	Used for ICW2, ICW3, or ICW4 in sequential order after ICW1 is written to port 0020h **ICW2** bits 7-3 = Address A0-A3 of base vector address for interrupt controller bits 2-0 = Reserved (should be 000) **ICW3** (for slave controller 00A1h) bits 7-3 = Reserved (should be 0000) bits 2-0 = 1 Slave ID **ICW4** bits 7-5 = Reserved (should be 000) bit 4 = 0 No special fully nested mode 1 Special fully nested mode bits 3-2 = Mode 00 Non buffered mode 01 Non buffered mode 10 Buffered mode/slave 11 Buffered mode/master bit 1 = 0 Normal EOI 1 Auto EOI bit 0 = 0 8085 mode 1 8080 / 8088 mode

Continued...

I/O Address	Read/Write Status	Description
0021h	R / W	PIC master interrupt mask register (OCW1) bit 7 = 0 Enable parallel printer interrupt bit 6 = 0 Enable diskette interrupt bit 5 = 0 Enable hard disk interrupt bit 4 = 0 Enable serial port 1 interrupt bit 3 = 0 Enable serial port 2 interrupt bit 2 = 0 Enable video interrupt bit 1 = 0 Enable kybd/pointing device/RTC interrupt bit 0 = 0 Enable interrupt timer
0021h	W	PIC OWC2 (if bits 4-3 = 0) bit 7 = Reserved bits 6-5 = 000 Rotate in automatic EOI mode (clear) 001 Nonspecific EOI 010 No operation 011 Specific EOI 100 Rotate in automatic EOI mode (set) 101 Rotate on nonspecific EOI command 110 Set priority command 111 Rotate on specific EOI command bits 4-3 = Reserved (should be 00) bits 2-0 = Interrupt request to which the command applies
0020h	R	PIC interrupt request and in-service registers programmed by OCW3 **Interrupt request register** bits 7-0 = 0 No active request for the corresponding interrupt line 1 Active request for the corresponding interrupt line **Interrupt in-service register** bits 7-0 = 0 Corresponding interrupt line not currently being serviced 1 Corresponding interrupt line is currently being serviced
0021h	W	PIC OCW3 (if bit 4 = 0, bit 3 = 1) bit 7 = Reserved (should 0) bits 6-5 = 00 No operation 01 No operation 10 Reset special mask 11 Set special mask bit 4 = Reserved (should be 0) bit = Reserved (should be 1) bit 2 = 0 No poll command 1 Poll command bits 1-0 = 00 No operation 01 Operation 10 Read interrupt request register on next read at port 0020 h 11 Read interrupt in-service register on next read at port 0020h

Continued...

I/O Address	Read/Write Status	Description
0022h	R / W	Chipsset Register Address
0023h	R / W	Chipsset Register Data
0040h	R / W	Programmable Interrupt Time read/write counter 0, keyboard controller channel 0
0041h	R / W	Programmer Interrupt Timer channel 1
0042h	R / W	Programmable Interrupt Timer miscellaneous register channel 2
0043h	W	Programmable Interrupt Timer mode port - control word register for counters 0 and 2 bits 7-0 = Counter select 00 Counter 0 select 01 Counter 1 select 10 Counter 2 select bits 5-4 = 00 Counter latch command 01 R / W counter, bits 0-7 only 10 R / W counter, bits 8-15 only 11 R / W counter, bits 0-7 first, then bits 8-15 bits 3-1 = Select mode 000 Mode 0 001 Mode 1 programmable one shot x10 Mode 2 rate generator x11 Mode 3 square wave generator 100 Mode 4 software-triggered strobe 101 Mode 5 hardware-triggered strobe bit 0 = 0 Binary counter is 16 bits 1 Binary counter decimal (BCD) counter
0048h	R / W	Programmable interrupt timer
0060h	R	Keyboard controller data port or keyboard input buffer
0060h	W	Keyboard or keyboard controller data output buffer

Continued...

I/O Address	Read/Write Status	Description
0064h	R	Keyboard controller read status bit 7 = 0 No parity error 1 Parity error on keyboard transmission bit 6 = 0 No timeout 1 Received timeout bit 5 = 0 No timeout 1 Keyboard transmission timeout bit 4 = 0 Keyboard inhibited 1 Keyboard not inhibited bit 3 = 0 Data 1 Command bit 2 = System flag status bit 1 = 0 Input buffer empty 1 Input buffer full bit 0 = 0 Output buffer empty 1 Output buffer full
0064h	W	Keyboard controller input buffer
0070h	R	CMOS RAM index register port and NMI mask bit 7 = 1 NMI disabled bits 6-0 = 0 CMOS RAM index
0071h	R / W	CMOS RAM data register port
0080h	R / W	Temporary storage for additional page register
0080h	R	Manufacturing diagnostic port (this port can access POST checkpoints)
0081h	R / W	DMA channel 2 address byte 2
0082h	R / W	DMA channel 2 address byte 2
0083h	R / W	DMA channel 1 address byte 2
0084h	R / W	Extra DMA page register
0085h	R / W	Extra DMA page register
0086h	R / W	Extra DMA page register
0087h	R / W	DMA channel 0 address byte 2
0088h	R / W	Extra DMA page register
0089h	R / W	DMA channel 6 address byte 2
008Ah	R / W	DMA channel 7 address byte 2
008Bh	R / W	DMA channel 5 address byte 2
008Ch	R / W	Extra DMA page register
008Dh	R / W	Extra DMA page register
008Eh	R / W	Extra DMA page register
008Fh	R / W	DMA refresh page register

Continued...

I/O Address	Read/Write Status	Description
00A0h - 00A1h are reserved for the slave programmable interrupt controller. The bit definitions are identical to those of addresses 0020h - 0021h except where indicated.		
00A0h	R / W	Programmable interrupt controller 2
00A1h	R / W	Programmable interrupt controller 2 mask bit 7 = 0 Reserved bit 6 = 0 Enable hard disk interrupt bit 5 = 0 Enable coprocessor execution interrupt bit 4 = 0 Enable mouse interrupt bits 3-2 = 0 Reserved bit 1 = 0 Enable redirect cascade bit 0 = 0 Enable real time clock interrupt
00C0h	R / W	DMA channel 4 memory address bytes 1 and 0 (low)
00C2h	R / W	DMA channel 4 transfer count bytes 1 and 0 (low)
00C4h	R / W	DMA channel 5 memory address bytes 1 and 0 (low)
00C6h	R / W	DMA channel 5 transfer count bytes 1 and 0 (low)
00C8h	R / W	DMA channel 6 memory address bytes 1 and 0 (low)
00CAh	R / W	DMA channel 6 transfer count bytes 1 and 0 (low)
00CCh	R / W	DMA channel 7 memory address bytes 1 and 0 (low)
00CEh	R / W	DMA channel 7 transfer count bytes 1 and 0 (low)
00D0h	R	Status register for DMA channels 4-7 bit 7 = 1 Channel 7 request bit 6 = 1 Channel 6 request bit 5 = 1 Channel 5 request bit 4 = 1 Channel 4 request bit 3 = 1 Terminal count on channel 7 bit 2 = 1 Terminal count on channel 6 bit 1 = 1 Terminal count on channel 5 bit 0 = 1 Terminal count on channel 4
00D0h	W	Command register for DMA channels 4-7 bit 7 = 0 DACK sense active low 1 DACK sense active high bit 6 = 0 DREQ sense active low 1 DREQ sense active high bit 5 = 0 Late write selection 1 Extended write selection bit 4 = 0 Fixed Priority 1 Rotating Priority bit 3 = 0 Normal Timing 1 Rotating Timing bit 2 = 0 Enable controller 1 Disable controller bit 1 = 0 Disable memory-to-memory transfer 1 Enable memory-to-memory transfer bit 0 = Reserved

Continued...

I/O Address	Read/Write Status	Description
00D2h	W	Write request register for DMA channels 4-7
00D4h	W	Write single mask register bit for DMA channels 4-7 bits 7-3 = 0 Reserved bit 2 = 0 Clear mask bit, 1 Set mask bit bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D6h	W	Mode register for DMA channels 4-7 bits 7-6 = 00 Demand mode 01 Single mode 10 Block mode 11 Cascade mode bit 5 = 0 Address increment select 1 Address decrement select bit 4 = 0 Disable auto initialization 1 Enable auto initialization bits 3-2 = Operation type 00 Verify operation 01 Write to memory 10 Read from memory 11 Reserved bits 1-0 = Channel select 00 Channel 4 01 Channel 5 10 Channel 6 11 Channel 7
00D8h	W	Clear byte pointer flip/flop for DMA channels 4-7
00DAh	R	Read Temporary Register for DMA channels 4-7
00DAh	W	Master Clear for DMA channels 4-7
00DCh	W	Clear mask register for DMA channels 4-7
00DEh	W	Write mask register for DMA channels 4-7
00F0h	W	Math coprocessor clear busy latch
00F1h	W	Math coprocessor reset
00F2h - 00FFh	R / W	Math coprocessor
0140h – 014Fh	R / W	SCSI Controller if installed
I/O addresses 0170h - 0177h are reserved for use with a secondary hard drive. See addresses 01F0h - 01F7h for bit definitions.		
0170h	R / W	Data register for hard drive 1
0171h	R	Error register for hard drive 1
0171h	W	Precomposition register for hard drive 1
0172h	R / W	Sector count - hard drive 1

Continued...

I/O Address	Read/Write Status	Description
0173h	R / W	Sector number for hard disk 1
0174h	R / W	Number of cylinders (low byte) for hard drive 1
0175h	R / W	Number of cylinders (high byte) for hard drive 1
0716h	R / W	Drive/head register for hard drive 1
0177h	R	Status register for hard drive 1
0177h	W	Command register for hard drive 1
01F0h	R / W	Data register base port for hard drive 0
01F1h	R	Error register for hard drive 0 **Diagnostic mode** bits 7-3 = Reserved bits 2-0 = Errors 0001 No errors 0010 Controller error 0011 Sector buffer error 0100 ECC device error 0101 Control processor error **Operation mode** bit 7 = Block 0 Bad block 1 Block not bad bit 6 = Error 0 No error 1 Uncorrectable ECC error bit 5 = Reserved bit 4 = ID 0 ID located 1 ID not located bit 3 = Reserved bit 2 = Command 0 Completed 1 Not completed bit 1 = Track 000 0 Not found 1 Found bit 0 = DRAM 0 Not found 1 Found (CP-3022 always 0)
01F1h	W	Write precomposition register for hard drive 0
01F2h	R / W	Sector count for hard disk 0
01F3h	R / W	Sector number for hard drive 0
01F4h	R / W	Number of cylinders (low byte) for hard drive 0
01F5h	R / W	Number of cylinders (high byte) for hard drive 0

Continued...

I/O Address	Read/Write Status	Description
01F6h	R / W	Drive/Head register for hard drive 0 bit 7 = 1 bit 6 = 0 bit 5 = 1 bit 4 = Drive select 0 First hard drive 1 Second hard drive bits 3-0 = Head select bits
01F7h	R	Status register for hard drive 0 bit 7 = 1 Controller is executing a command bit 6 = 1 Drive is ready bit 5 = 1 Write fault bit 4 = 1 Seek operation complete bit 3 = 1 Sector buffer requires servicing bit 2 = 1 Disk data read completed successfully bit 1 = Index (is set to 1 at each disk revolution) bit 0 = 1 Previous command ended with error
01F7h	W	Command register for hard drive 0
0200h - 020Fh	R / W	Game controller ports
0201h	R / W	I/O data - game port
0220h – 022Fh	R / W	Soundport AD1816 reserved
I/O addresses 0278h - 027Ah are reserved for use with parallel port 2. See the bit definitions for addresses 0378h - 037Ah.		
0278h	R / W	Data port for parallel port 2
0279h	R	Status port for parallel port 2
0279h	W	PnP Address register (only for PnP devices)
027Ah	R / W	Control port for parallel port 2
02B0h – 02BFh	R / W	Digital I/O for Latch, WDOG, Control
I/O addresses 02E8h - 02EFh are reserved for use with serial port 4. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02E8h	W	Transmitter holding register for serial port 4
02E8h	R	Receive buffer register for serial port 4
02E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02E9h	R / W	Baud rate divisor (high byte) when DLAB = 1
02E9h	R / W	Interrupt enable register when DLAB = 0
02EAh	R	Interrupt identification register for serial port 4
02EBh	R / W	Line control register for serial port 4
02ECh	R / W	Modem control register for serial port 4
02EDh	R	Line status register for serial port 4
02EEh	R	Modem status register for serial port 4
02EFh	R / W	Scratch register for serial port 4 (used for diagnostics)

Continued...

I/O Address	Read/Write Status	Description
I/O addresses 02F8h - 02FFh are reserved for use with serial port 2. See the bit definitions for I/O addresses 03F8h - 03FFh.		
02F8h	W	Transmitter holding register for serial port 2
02F8h	R	Receive buffer register for serial port 2
02F8h	R / W	Baud rate divisor (low byte) when DLAB = 1
02F9h	R / W	Baud rate divisor (high byte) when DLAB = 1
02F9h	R / W	Interrupt enable register when DLAB = 0
02FAh	R	Interrupt identification register for serial port 2
02FBh	R / W	Line control register for serial port 2
02FCh	R / W	Modem control register for serial port 2
02FDh	R	Line status register for serial port 2
02FEh	R	Modem status register for serial port 2
02FFh	R / W	Scratch register for serial port 2 (used for diagnostics)
0300h – 031Fh	R / W	LAN controller if installed
I/O addresses 0372h - 0377h are reserved for use with a secondary diskette controller. See the bit definitions for 03F2h - 03F7h.		
0372h	W	Digital output register for secondary diskette drive controller
0374h	R	Status register for secondary diskette drive controller
0375h	R / W	Data register for secondary diskette drive controller
0376h	R / W	Control register for secondary diskette drive controller
0377h	R	Digital input register for secondary diskette drive controller
0377h	W	Select register for secondary diskette data transfer rate
0378h	R / W	Data port for parallel port 1
0379h	R	Status port for parallel port 1 bit 7 = 0 Busy bit 6 = 0 Acknowledge bit 5 = 1 Out of paper bit 4 = 1 Printer is selected bit 3 = 0 Error bit 2 = 0 IRQ has occurred bit 1-0 = Reserved

Continued...

I/O Address	Read/Write Status	Description
037Ah	R / W	Control port for parallel port 1 bits 7-5 = Reserved bit 4 = 1 Enable IRQ bit 3 = 1 Select printer bit 2 = 0 Initialize printer bit 1 = 1 Automatic line feed bit 0 = 1 Strobe
03B0h - 03B8h	R / W	Various video registers
I/O addresses 03BCh - 03BEh are reserved for use with parallel port 3. See the bit definitions for addresses 0378h - 037Ah.		
03BCh	R / W	Data port - parallel port 3
03BDh	R / W	Status port - parallel port 3
03BEh	R / W	Control port - parallel port 3
03C0h - 03CFh	R / W	Video subsystem (EGA/VGA)
03C2h - 03D9h	R / W	Various CGA and CRTC registers
03E0h	R / W	PCCARD Address select
03E1h	R / W	PCCARD Data transfer with 365SL controller
I/O addresses 03E8h - 03EFh are reserved for use with serial port 3. See the bit definitions for I/O addresses 03F8h - 03FFh.		
03E8h	W	Transmitter holding register for serial port 3
03E8h	R	Receive buffer register for serial port 3
03E8h	R / W	Baud rate divisor (low byte) when DLAB = 1
03E9h	R / W	Baud rate divisor (high byte) when DLAB = 1
03E9h	R / W	Interrupt enable register when DLAB = 0
03EAh	R	Interrupt identification register for serial port 3
03EBh	R / W	Line control register for serial port 3
03ECh	R / W	Modem control register for serial port 3
03EDh	R	Line status register for serial port 3
03EEh	R	Modem status register for serial port 3
03EFh	R / W	Scratch register for serial port 3 (used for diagnostics)
03F2h	W	Digital output register for primary diskette drive controller bits 7-6 = 0 Reserved bit 5 = 1 Enable drive 1 motor bit 4 = 1 Enable drive 0 motor bit 3 = 1 Enable diskette DMA bit 2 = 0 Reset controller bit 1 = 0 Reserved bit 0 = 0 Select drive 0 1 Select drive 1

Continued...

I/O Address	Read/Write Status	Description
03F4h	R	Status register for primary diskette drive controller bit 7 = 1 Data register is ready bit 6 = 0 Transfer from system to controller 1 Transfer from controller to system bit 5 = 1 Non-DMA mode bit 4 = 1 Diskette drive controller is busy bits 3-2 = Reserved bit 1 = 1 Drive 1 is busy bit 0 = 1 Drive 0 is busy
03F5h	R / W	Data register for primary diskette drive controller
03F6h	R	Control port for primary diskette drive controller bits 7-4 = Reserved bit 3 = 0 Reduce write current 1 Head select enable bit 2 = 0 Disable diskette drive reset 1 Enable diskette drive reset bit 1 = 0 Disable diskette drive initialization 1 Enable diskette drive initialization bit 0 = Reserved
03F7h	R	Digital input register for primary diskette drive controller bit 7 = 1 Diskette drive line change bit 6 = 1 Write gate bit 5 = Head select 3 / reduced write current bit 4 = Head select 2 bit 3 = Head select 1 bit 2 = Head select 0 bit 1 = Drive 1 select bit 0 = Drive 0 select
03F7h	W	Select register for primary diskette data transfer rate bits 7-2 = Reserved bits 1-0 = 00 500 Kbs mode 01 300 Kbs mode 10 250 Kbs mode 11 Reserved
I/O addresses 03F8h - 03FFh are reserved for use with serial port 1. The bit definitions for these addresses also apply to serial ports 2, 3, and 4.		
03F8h	W	Transmitter holding register for serial port 1 - Contains the character to be sent. Bit 0, the least significant bit, is the first bit sent. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0
03F8h	R	Receive buffer register for serial port 1 - Contains the character to be received. Bit 0, the least significant bit, is the first bit received. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 0

Continued...

I/O Address	Read/Write Status	Description
03F8h	R / W	Baud rate divisor (low byte) - This byte along with the high byte (03F9h) store the data transmission rate divisor. bits 7-0 = Data bits 0-7 when the Divisor Latch Access Bit (DLAB) is 1
03F9h	R / W	Baud rate divisor (high byte) - This byte along with the low byte (03F8h) store the data transmission rate divisor. bits 7-0 = Bits 8-15 when DLAB = 1
03F9h	R / W	Interrupt enable register bits 7-4 = Reserved bit 3 = 1 Modem status interrupt enable bit 2 = 1 Receiver line status interrupt enable bit 1 = 1 Transmitter holding register empty interrupt enable bit 0 = 1 Received data available interrupt enable when DLAB = 0
03FAh	R	Interrupt identification register - serial port 1 bits 7-3 = Reserved bits 2-1 = Identify interrupt with highest priority 00 Modem status interrupt (4th priority) 01 Transmitter holding register empty (3rd priority) 10 Received data available (2nd priority) 11 Receiver line status interrupt (1st priority) bit 0 = 0 Interrupt pending (register contents can be used as a pointer to interrupt service routine) 1 No interrupt pending
03FBh	R / W	Line control register - serial port 1 bit 7 = Divisor Latch Access (DLAB) 0 Access receiver buffer, transmitter holding register, and interrupt enable register 1 Access divisor latch bit 6 = 1 Set break enable. Forces serial output to spacing state and remains there bit 5 = Stick parity bit 4 = Even parity select bit 3 = Parity enable bit 2 = Number of stop bits bit 1 = Word length 00 5-bit word length 01 6-bit word length 10 7-bit word length 11 8-bit word length
03FCh	R / W	Modem control register - serial port 1 bits 7-5 = Reserved bit 4 = 1 Loopback mode for diagnostic testing of serial port. bit 3 = 1 User-defined output 2 bit 2 = 1 User-defined output 1 bit 1 = Force Request To Send active bit 0 = Force Data Terminal Ready active

Continued...

I/O Address	Read/Write Status	Description
03FDh	R	Line status register - serial port 1 bit 7 = Reserved bit 6 = 1 Transmitting shift and holding registers empty bit 5 = 1 Transmitter shift register empty bit 4 = 1 Break interrupt bit 3 = 1 Framing error bit 2 = 1 Overrun error bit 0 = 1 Data ready
03FEh	R	Modem status register - serial port 1 bit 7 = 1 Data Carrier Detect bit 6 = 1 Ring Indicator bit 5 = 1 Data Set Ready bit 4 = 1 Clear To Send bit 3 = 1 Delta Data Carrier bit 2 = 1 Trailing Edge Ring Indicator bit 1 = 1 Delta Data Set Ready bit 0 = 1 Delta Clear To Send
03FFh	R / W	Scratch register - serial port 1 (used for diagnostics)
0A79h	W	PnP Data write register (only for PnP devices)

4.9 BIOS Data Area Definitions

The BIOS Data Area is an area within system RAM that contains information about the system environment. System environment information includes definitions associated with hard disks, diskette drives, keyboard, video, as well as other BIOS functions. This area is created when the system is first powered on. It occupies a 256-byte area from 0400h - 04FFh. The following table lists the contents of the BIOS data area locations in offset order starting from segment address 40:00h.

Location	Description
00h - 07h	I/O addresses for up to 4 serial ports
08h - 0Dh	I/O addresses for up to 3 parallel ports
0Eh - 0Fh	Segment address of extended data address
10h - 11h	Equipment list bits 15-14 = Number of parallel printer adapters 00 = Not installed 01 = One 10 = Two 11 = Three bits 13-12 = Reserved bits 11-9 = Number of serial adapters 00 = Not installed 001 = One 010 = Two 011 = Three 100 = Four bit 8 = Reserved bits 7-6 = Number of diskette drives 00 = One drive 01 = Two drives bits 5-4 = Initial video mode 00 = EGA or PGA 01 = 40 x 25 color 10 = 80 x 25 color 11 = 80 x 25 monochrome bit 3 = Reserved bit 2 = (1) Pointing device present bit 1 = (1) Math coprocessor present bit 0 = (1) Diskette drive present
12h	Reserved for port testing by manufacturer bits 7-1 = Reserved bit 0 = (0) Non-test mode (1) Test mode
13h	Memory size in kilobytes - low byte
14h	Memory size in kilobytes - high byte

Continued...

BIOS Data Area Definitions Continued...

Location	Description
15h - 16h	Reserved
17h	Keyboard Shift Qualifier States bit 7 = Insert mode bit 6 = CAPS lock bit 5 = Numlock bit 4 = Scroll Lock bit 3 = Either Alt key bit 2 = Either control key bit 1 = Left Shift key bit 0 = Right shift key 0 = not set / 1 = set
18h	Keyboard Toggle Key States bit 7 = (1) Insert held down bit 6 = (1) CAPS lock held down bit 5 = (1) Num Lock held down bit 4 = (1) Scroll Lock held down bit 3 = (1) Control+Num Lock held down bit 2 = (1) Sys Re held down bit 1 = (1) Left Alt held down bit 0 = (1) Left Control held down
19h	Scratch area for input from Alt key and numeric keypad
1Ah - 1Bh	Pointer to next character in keyboard buffer
1Ch - 1Dh	Pointer to last character in keyboard buffer
1Eh - 3Dh	Keyboard Buffer. Consists of 16 word entries.
3Eh	Diskette Drive Recalibration Flag bit 7 = (1) Diskette hardware interrupt occurred bits 6-4 = Not used bits 3-2 = Reserved bit 1 = (0) Recalibrate drive B bit 0 = (0) Recalibrate drive A

Continued...

BIOS Data Area Definitions Continued...

Location	Description
3Fh	Diskette Drive Motor Status bit 7 = Current operation 0 = Write or Format 1 = Read or Verify bit 6 = Reserved bits 5-4 = Drive Select 00 = Drive A 01 = Drive B bits 3-2 = Reserved 0 = Disable 1 = Enabled bit 1 = Drive B Motor Status 0 = Off 1 = On bit 1 = Drive A Motor Status 0 = Off 1 = On
40h	Diskette Drive Motor Timeout Disk drive motor is powered off when the value via the INT 08h timer interrupt reaches 0.
41h	Diskette Drive Status bit 7 = Drive Ready 0 = Ready 1 = Not ready bit 6 = Seek Error 0 = No error 1= Error occurred bit 5 = Controller operation 0 = Working 1 = Failed bits 4-0 = Error Codes 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 06h = Diskette change line active (door opened) 08h = DMA overrun error 09h = Data boundary error 0Ch = Unknown media type 10h = ECC or CRC error 20h = Controller failure 40h = Seek operation failure 80h = Timeout
42h - 48h	Diskette Controller Status Bytes
49h	Video Mode Setting
4Ah - 4Bh	Number of Columns on screen
4Ch - 4Dh	Size of Current Page, in bytes
4Eh - 4Fh	Address of Current Page

Continued...

BIOS Data Area Definitions Continued...

Location	Description
50h - 5Fh	Position of cursor for each video page. Current cursor position is stored two bytes per page. First byte specifies the column, the second byte specifies the row.
60h - 61h	Start and end lines for 6845-compatible cursor type. 60h = starting scan line, 61h = ending scan line.
62h	Current Video Display Page
63h - 64h	6845-compatible I/O port address for current mode 3B4h = Monochrome 3D4h = Color
65h	Register for current mode select
66h	Current palette setting
67 - 6Ah	Address of adapter ROM
6Bh	Last interrupt the occurred
6Ch - 6Dh	Low word of timer count
6Eh - 6Fh	High word of timer count
70h	Timer count for 24-hour rollover flag
71h	Break key flag
72h - 73h	Reset flag 1243h = Soft reset. Memory test is bypassed.
74h	Status of last hard disk operation 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 05h = Reset failed 08h = DMA overrun error 09h = Data boundary error 0Ah = Bad sector flag selected 0Bh = Bad track detected 0Dh = Invalid number of sectors on format 0Eh = Control data address mark detected 0Fh = DMA arbitration level out of range 10h = ECC or CRC error 11h = Data error corrected by ECC 20h = Controller failure 40h = Seek operation failure 80h = Timeout AAh = Drive not ready BBh = Undefined error occurred CCh = Write fault on selected drive E0h = Status error or error register = 0 FFh = Sense operation failed
75h	Number of hard drives
76h - 77h	Work area for hard disk

Continued...

BIOS Data Area Definitions Continued...

Location	Description
78h - 7Bh	Default parallel port timeout values
7Dh - 7Fh	Default serial port timeout values
80h - 81h	Pointer to start of keyboard buffer
82h - 83h	Pointer to end of keyboard buffer
84h - 88h	Reserved for EGA/VGA BIOS
8Ah	Reserved
8Bh	Diskette drive data transfer rate information bits 7-5 = Data rate on last operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 5-4 = Last drive step rate selected bits 3-2 = Data transfer rate at start of operation 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bits 1-0 = Reserved
8Ch	Copy of hard status register
8Dh	Copy of hard drive error register
8Eh	Hard drive interrupt flag
8Fh	Diskette controller information bit 7 = Reserved bit 6 = (1) Drive confirmed for drive B bit 5 = (1) Drive B is multi-rate bit 4 = (1) Drive B supports line change bit 3 = Reserved bit 2 = (1) Drive determined for drive A bit 1 = (1) Drive B is multi-rate bit 0 = (1) Drive B supports line change
90h - 91h	Media type for drives bits 7-6 = Data transfer rate 00 = 500 KBS 01 = 300 KBS 10 = 250 KBS bit 5 = (1) Double stepping required when 360K diskette inserted into 1.2MB drive bit 4 = (1) Known media is in drive bit 3 = Reserved bits 2-0 = Definitions upon return to user applications 000 = Testing 360K in 360K drive 001 = Testing 360K in 1.2 MB drive 010 = Testing 1.2 MB in 1.2 MB drive 011 = Confirmed 360K in 360K drive 100 = Confirmed 360K in 1.2 MB 101 = Confirmed 1.2 MB in 1.2 MB drive 111 = 720K in 720K drive or 1.44 MB in 1.44 MB drive

Continued...

BIOS Data Area Definitions Continued...

Location	Description
92h - 93h	Scratch area for diskette media. Low byte for drive A, high byte for drive B.
94h - 95h	Current track number for both drives. Low byte for drive A, high byte for drive B.
96h	Keyboard Status bit 7 = (1) Read ID bit 6 = (1) Last code was first ID bit 5 = (1) Force to Num Lock after read ID bit 4 = (1) Enhanced keyboard installed bit 3 = (1) Right ALT key active bit 2 = (1) Right Control key active bit 1 = (1) Last code was E0h bit 0 = (1) Last code was E1h
97h	Keyboard Status bit 7 = (1) Keyboard error bit 6 = (1) Updating LEDs bit 5 = (1) Resend code received bit 4 = (1) Acknowledge received bit 3 = Reserved bit 2 = (1) Caps lock LED state bit 1 = (1) Num lock LED state bit 0 = (1) Scroll lock LED state
98h - 99h	Offset address of user wait flag
9Ah - 9Bh	Segment address of user wait flag
9Ch - 9Dh	Wait count, in microseconds (low word)
9Eh - 9Fh	Wait count, in microseconds (high word)
A0h	Wait active flag bit 7 = (1) Time has elapsed bits 6-1 = Reserved bit 0 = (1) INT 15h, AH = 86h occurred
A1h - A7h	Reserved
A8h - ABh	Pointer to video parameters and overrides
ACh - FFh	Reserved
100h	Print screen status byte

4.9.1.1 Compatibility Service Table

In order to ensure compatibility with industry-standard memory locations for interrupt service routines and miscellaneous tabular data, the BIOS maintains tables and jump vectors.

Location	Description
FE05Bh	Entry Point for POST
FE2C3h	Entry point for INT 02h (NMI service routine)
FE3FEh	Entry point for INT 13h (Diskette Drive Services)
FE401h	Hard Drive Parameters Table
FE6F1h	Entry point for INT 19h (Bootstrap Loader routine)
FE6F5h	System Configuration Table
FE739h	Entry point for INT 14h (Serial Communications)
FE82Eh	Entry point for INT 16h (Keyboard Services)
FE897h	Entry point for INT 09h (Keyboard Services)
FEC59h	Entry point for INT 13h (Diskette Drive Services)
FEF57h	Entry point for INT OEh (Diskette Hardware Interrupt)
FEFC7h	Diskette Drive Parameters Table
FEFD2h	Entry point for INT 17h (Parallel Printer Services)
FF065h	Entry point for INT 10h (CGA Video Services)
FF0A4h	Video Parameter Table (6845 Data Table - CGA)
FF841h	Entry point for INT 12h (Memory Size Service)
FF84Dh	Entry point for INT 11h (Equipment List Service)
FF859h	Entry point for INT 15h (System Services)
Location	**Description**
FFA6Eh	Video graphics and text mode tables
FFE6Eh	Entry point for INT 1Ah (Time-of-Day Service)
FFEA5h	Entry Point for INT 08h (System Timer Service)
FFEF3h	Vector offset table loaded by POST
FFF53h	Dummy Interrupt routine IRET Instruction
FFF54h	Entry point for INT 05h (Print Screen Service)
FFFF0h	Entry point for Power-on
FFFF5h	BIOS Build Date (in ASCII)
FFFFEh	BIOS ID

4.10 VGA, LCD

4.10.1 VGA / LCD Controller C&T65554 and C&T65555

The 65554 / 65555 HiQV64 Flatpanel/CRT VGA controller

- High integrated design (flatpanel/CRT VGA controller, RAMDAC, clock synthesizer)
- PCI 32bit Bus with 33Mhz
- Flexible display memory configurations 2Mbyte standard, 4Mbyte optional
- Videoport ZV, YUV 16Bit Input
- Integrated programmable linear address feature accelerates GUI performance
- Hardware windows acceleration, HW Stretching/Scailing, Auto Panning Support
- 44k BIOS for CRT/FP/Sim FP, Multiple refreshrates, up to 16 Panels in one BIOS, INT15 Hooks
- Mixed 3.3 V / 5.0 V +/- 10 % Operation
- Interface to 3 channels PAL or NTSC videosources with 30 img/sec capturing
- YUV to RGB conversion with zooming up to 8x
- Supports panel resolutions up to 1280 x 1024, including 800x600 and 1024x768
- Supports non-interlaced CRT monitors with resolutions up to 1600 x 1280
- Truecolor / HiColor display capability with flatpanels and CRT monitors up to 1024 x 768 resolution
- Direct interface to Color and Monochrome Dual Drive (DD) and Single Drive (SS) panels (supports 8, 9, 12, 15, 16, 18, 24 and 36 Bit data interfaces)
- Advanced power management features minimize power consumption during:
  - Normal operation
  - Standby (Sleep) modes
  - Panel-Off Power-Saving Mode
- Flexible onboard Activity Timer facilitates ordered shut-down of the display system
- Power Sequencing control outputs regulate application of Bias voltage, +5 V to the panel and +12 V to the inverter for backlight operation
- SMARTMAP™ intelligent color to gray scale conversion enhances text legibility
- Text enhancement feature improves white text contrast on flatpanel displays
- Fully Compatible with IBM™ VGA

4.10.2 VGA / LCD BIOS for 65555 and (69000 not supported)

VGA BIOS

The 65555 and 69000 VGA BIOS (hereafter referred to as 69000 BIOS) is an enhanced, high performance BIOS that is used with the 69000 VGA Flat Panel/CRT Controller to provide an integrated Flat panel VGA solution. The BIOS is optimized for 69000 VGA Flat Panel/CRT Controller and provides:

Full compatibility with the IBM VGA BIOS
Support for monochrome LCD, 640x480, 800x600, 1024x768 and 1280x1024 TFT or STN displays.
Optional support for other displays.
Supports VESA BIOS Extensions, including VBE 2.0, VBE/DDC 1.0, and VBE/PM 1.0.
Supports either VESA local bus or PCI bus
Extended BIOS functions which offer easy access to 69000 control ler features and capabilities
Support for simultaneous display
44K BIOS supports 8 panels
48K BIOS supports 16 panels

4.10.3 Memory 65554/65555/CRT/TFT Panels

Hor. Resol.	Vert. Resol.	Color bpp	Refr. Hz	DCLK Mhz	MEM kByte	Cursor kByte	FB/C kByte	FB/M kByte	Video Input kByte	Total with Video	Total w/o Video
640	480	8	60	25.175	300	4.2	0	0	300	604	304
640	480	8	72	31.500	300	4.2	0	0	300	604	304
640	480	8	75	31.500	300	4.2	0	0	300	604	304
640	480	8	85	36.000	300	4.2	0	0	300	604	304
640	480	16	60	25.175	600	4.2	0	0	300	904	604
640	480	16	72	31.500	600	4.2	0	0	300	904	604
640	480	16	75	31.500	600	4.2	0	0	300	904	604
640	480	16	85	36.000	600	4.2	0	0	300	904	604
640	480	24	60	25.175	900	4.2	0	0	300	1204	904
640	480	24	72	31.500	900	4.2	0	0	300	1204	904
640	480	24	75	31.500	900	4.2	0	0	300	1204	904
640	480	24	85	36.000	900	4.2	0	0	300	1204	904
800	600	8	60	40.000	469	4.2	0	0	300	773	473
800	600	8	72	50.000	469	4.2	0	0	300	773	473
800	600	8	75	49.500	469	4.2	0	0	300	773	473
800	600	8	85	56.250	469	4.2	0	0	300	773	473
800	600	16	60	40.000	938	4.2	0	0	300	1242	942
800	600	16	72	50.000	938	4.2	0	0	300	1242	942
800	600	16	75	49.500	938	4.2	0	0	300	1242	942
800	600	16	85	56.250	938	4.2	0	0	300	1242	942
800	600	24	60	40.000	1406	4.2	0	0	300	1710	1410
800	600	24	72	50.000	1406	4.2	0	0	300	1710	1410
800	600	24	75	49.500	1406	4.2	0	0	300	1710	1410
800	600	24	85	56.250	1406	4.2	0	0	300	1710	1410
1024	768	16	60	65.000	1536	4.2	0	0	300	1840	1540
1024	768	16	70	75.000	1536	4.2	0	0	300	1840	1540
1024	768	16	75	78.750	1536	4.2	0	0	300	1840	1540
1024	768	16	85	94.500	1536	4.2	0	0	300	1840	1540
1024	768	24	60	65.000	2304	4.2	0	0	300	2608	2308
1024	768	24	72	75.000	2304	4.2	0	0	300	2608	2308
1024	768	24	75	78.750	2304	4.2	0	0	300	2608	2308
1024	768	24	85	94.500	2304	4.2	0	0	300	2608	2308
1280	1024	16	60	108.0	2560	4.2	0	0	300	2864	2564
1280	1024	16	70	128.0	2560	4.2	0	0	300	2864	2564
1280	1024	16	75	135.0	2560	4.2	0	0	300	2864	2564
1280	1024	16	85	157.5	2560	4.2	0	0	300	2864	2564
1280	1024	24	60	108.0	3840	4.2	0	0	300	4144!	3844
1280	1024	24	72	128.0	3840	4.2	0	0	300	4144!	3844
1280	1024	24	75	135.0	3840	4.2	0	0	300	4144!	3844
1280	1024	24	85	157.5	3840	4.2	0	0	300	4144!	3844

! means not possible resolution with the 4Mb Video RAM

4.10.4 Memory 65554/65555 Color STN-DD Panels

Hor. Resol.	Vert. Resol.	Color bpp	Refr. Hz	DCLK Mhz	MEM kByte	Cursor kByte	FB/C kByte	FB/M kByte	Video Input kByte	Total with Video	Total w/o Video
640	480	8	60	25.175	300	4.2	120	0	300	724	424
640	480	8	72	31.500	300	4.2	120	0	300	724	424
640	480	8	75	31.500	300	4.2	120	0	300	724	424
640	480	8	85	36.000	300	4.2	120	0	300	724	424
640	480	16	60	25.175	600	4.2	120	0	300	1024	724
640	480	16	72	31.500	600	4.2	120	0	300	1024	724
640	480	16	75	31.500	600	4.2	120	0	300	1024	724
640	480	16	85	36.000	600	4.2	120	0	300	1024	724
640	480	24	60	25.175	900	4.2	120	0	300	1324	1024
640	480	24	72	31.500	900	4.2	120	0	300	1324	1024
640	480	24	75	31.500	900	4.2	120	0	300	1324	1024
640	480	24	85	36.000	900	4.2	120	0	300	1324	1024
800	600	8	60	40.000	469	4.2	188	0	300	960	660
800	600	8	72	50.000	469	4.2	188	0	300	960	660
800	600	8	75	49.500	469	4.2	188	0	300	960	660
800	600	8	85	56.250	469	4.2	188	0	300	960	660
800	600	16	60	40.000	938	4.2	188	0	300	1429	1129
800	600	16	72	50.000	938	4.2	188	0	300	1429	1129
800	600	16	75	49.500	938	4.2	188	0	300	1429	1129
800	600	16	85	56.250	938	4.2	188	0	300	1429	1129
800	600	24	60	40.000	1406	4.2	188	0	300	1898	1598
800	600	24	72	50.000	1406	4.2	188	0	300	1898	1598
800	600	24	75	49.500	1406	4.2	188	0	300	1898	1598
800	600	24	85	56.250	1406	4.2	188	0	300	1898	1598
1024	768	16	60	65.000	1536	4.2	307	0	300	2147	1847
1024	768	16	70	75.000	1536	4.2	307	0	300	2147	1847
1024	768	16	75	78.750	1536	4.2	307	0	300	2147	1847
1024	768	16	85	94.500	1536	4.2	307	0	300	2147	1847
1024	768	24	60	65.000	2304	4.2	307	0	300	2915	2615
1024	768	24	72	75.000	2304	4.2	307	0	300	2915	2615
1024	768	24	75	78.750	2304	4.2	307	0	300	2915	2615
1024	768	24	85	94.500	2304	4.2	307	0	300	2915	2615
1280	1024	16	60	108.0	2560	4.2	512	0	300	3376	3676
1280	1024	16	70	128.0	2560	4.2	512	0	300	3376	3676
1280	1024	16	75	135.0	2560	4.2	512	0	300	3376	3676
1280	1024	16	85	157.5	2560	4.2	512	0	300	3376	3676
1280	1024	24	60	108.0	3840	4.2	512	0	300	4656!	4356!
1280	1024	24	72	128.0	3840	4.2	512	0	300	4656!	4356!
1280	1024	24	75	135.0	3840	4.2	512	0	300	4656!	4356!
1280	1024	24	85	157.5	3840	4.2	512	0	300	4656!	4356!

! means not possible resolution with the 4Mb Video RAM

4.10.5 Memory 65554/65555 Mono STN-DD Panels

Hor. Resol.	Vert. Resol.	Color bpp	Refr. Hz	DCLK Mhz	MEM kByte	Cursor kByte	FB/C kByte	FB/M kByte	Video Input kByte	Total with Video	Total w/o Video
640	480	8	60	25.175	300	4.2	0	38	300	642	342
640	480	8	72	31.500	300	4.2	0	38	300	642	342
640	480	8	75	31.500	300	4.2	0	38	300	642	342
640	480	8	85	36.000	300	4.2	0	38	300	642	342
640	480	16	60	25.175	600	4.2	0	38	300	942	642
640	480	16	72	31.500	600	4.2	0	38	300	942	642
640	480	16	75	31.500	600	4.2	0	38	300	942	642
640	480	16	85	36.000	600	4.2	0	38	300	942	642
640	480	24	60	25.175	900	4.2	0	38	300	1242	942
640	480	24	72	31.500	900	4.2	0	38	300	1242	942
640	480	24	75	31.500	900	4.2	0	38	300	1242	942
640	480	24	85	36.000	900	4.2	0	38	300	1242	942
800	600	8	60	40.000	469	4.2	0	59	300	832	532
800	600	8	72	50.000	469	4.2	0	59	300	832	532
800	600	8	75	49.500	469	4.2	0	59	300	832	532
800	600	8	85	56.250	469	4.2	0	59	300	832	532
800	600	16	60	40.000	938	4.2	0	59	300	1300	1000
800	600	16	72	50.000	938	4.2	0	59	300	1300	1000
800	600	16	75	49.500	938	4.2	0	59	300	1300	1000
800	600	16	85	56.250	938	4.2	0	59	300	1300	1000
800	600	24	60	40.000	1406	4.2	0	59	300	1769	1469
800	600	24	72	50.000	1406	4.2	0	59	300	1769	1469
800	600	24	75	49.500	1406	4.2	0	59	300	1769	1469
800	600	24	85	56.250	1406	4.2	0	59	300	1769	1469

! means not possible resolution with the 4Mb Video RAM

4.10.6 Supported Standard VGA Modes

Mode:	Type:	Colors:	CRT:	Text:	Graphic:	DRAM:	Monitor:	Refresh/HR:
0,1	Text	16	ABC	40 x 25	320 x 200	256k	CGA	70 Hz
2,3	Text	16	ABC	80 x 25	640 x 200	256k	CGA	70 Hz
4,5	Graphic	4	ABC	40 x 25	320 x 200	256k	CGA	70 Hz
6	Graphic	2	ABC	80 x 25	640 x 200	256k	CGA	70 Hz
7+	Text	Mono	ABC	80 x 25	720 x 350	256k	HGC	70 Hz
D	Planar	16	ABC	40 x 25	320 x 200	256k	CGA	70 Hz
E	Planar	16	ABC	80 x 25	640 x 200	256k	CGA	70 Hz
F	Planar	Mono	ABC	80 x 25	640 x 350	256k	EGA	70 Hz
10	Planar	16	ABC	80 x 25	640 x 350	256k	EGA	70 Hz
11	Planar	2	ABC	80 x 30	640 x 480	256k	VGA	60 Hz
12/12+	Planar	16	ABC/BC	80 x 30	640 x 480	256k	VGA	60 Hz/72Hz
13	Planar	256	ABC	40 x 25	320 x 200	256k	CGA	70 Hz (not 8 Bit Bus)
20	4 Bit Lin	16	ABC	80 x 30	640 x 480	512k	VGA	60 Hz
22	4 Bit Lin	16	BC	100 x 37	800 x 600	512k	SVGA	60 Hz
30	8 Bit Lin	256	ABC	80 x 30	640 x 480	512k	VGA	60 Hz/72 Hz
32	8 Bit Lin	256	BC	100 x 37	800 x 600	512k	SVGA	60 Hz/72 Hz
60	Text	16	ABC	132 x 25	1056 x 400	256k	MGA	68 Hz
61	Text	16	ABC	132 x 50	1056 x 400	256k	MGA	68 Hz
72	Planar	16	C	128 x 48	1024 x 768	512k	HVGA	60 Hz
79	Packed	256	ABC	80 x 30	640 x 480	512k	VGA	72 Hz
7C	Packed	256	BC	100 x 37	800 x 600	512k	SVGA	72 Hz

24	4 Bit Lin	16	C	128 x 48	1024 x 768	1024k	HiVGA	60 Hz
26	4 Bit Lin	16	BC	128 x 48	1024 x 768	1024k	HiVGA	43 Hz
34	8 Bit Lin	256	C	128 x 48	1024 x 768	1024k	HiVGA	60 Hz
36	8 Bit Lin	256	BC	128 x 48	1024 x 768	1024k	HiVGA	43 Hz
40	15 Bit Lin	32k	ABC	80 x 30	640 x 480	1024k	VGA	60 Hz
41	16 Bit Lin	64k	ABC	80 x 30	640 x 480	1024k	VGA	60 Hz
7E	Packed	256	C	128 x 48	1024 x 768	1024k	HiVGA	60 Hz

A = PS/2 fixed frequency analog monitor;
B = Multifrequency CRT monitor like NEC Multisynch 3D or eq.
C = Nanao/EIZO 9070, NEC Multisynch 5D, or eq.

4.10.7 VGA CRT/LCD Display Driver

The purpose of the enclosed software drivers is to take advantage of the extended features of the 65554VGA controller. These capabilities include:

- Resolutions up to 1600 x 1280 in graphics modes
- Resolution up to 1024 x 768 in graphics modes at True Color
- 132 columns text mode in 16 colors

Our software drivers and utilities support the following applications and environments:

Program	Version
Windows	3.1, 95, NT3.5, NT4.0

The Windows drivers included in this packages have special features which are described in the Windows section of this manual:

- Multimedia extensions
- Big cursor support
- Panning drivers

4.10.7.1 65554/65555 HiQV64 VGA Driver Resolutions

Date: 8.97

Application:	Resolution:	Colors:	Videomemory:
Windows 3.1	640 x 480	16,256,32k,64k,16M	2MByte
	800 x 600	16,256,32k,64k,16M	2MByte
	1024 x 768	16,256,32k,64k	2MByte
	1280 x 1024	16,256	2MByte
Windows 3.1	640 x 480	16,256,32k,64k,16M	4MByte
	800 x 600	16,256,32k,64k,16M	4MByte
	1024 x 768	16,256,32k,64k,16M	4MByte
	1280 x 1024	16,256,32k,64k	4MByte
Windows 95	640 x 480	16,256,32k,64k,16M	2MByte
	800 x 600	16,256,32k,64k,16M	2MByte
	1024 x 768	16,256,32k,64k	2MByte
	1280 x 1024	16,256	2MByte
Windows 95	640 x 480	16,256,32k,64k,16M	4MByte
	800 x 600	16,256,32k,64k,16M	4MByte
	1024 x 768	16,256,32k,64k,16M	4MByte
	1280 x 1024	16,256,32k,64k	4MByte
	1600 x 1280	16,256	4MByte
NT4.0	640 x 480	16,256,32k,64k,16M	2MByte
	800 x 600	16,256,32k,64k	2MByte
	1024 x 768	16,256	2MByte
	1280 x 1024	16	2MByte
NT4.0	640 x 480	16,256,32k,64k,16M	4MByte
	800 x 600	16,256,32k,64k,16M	4MByte
	1024 x 768	16,256,32k,64k,16M	4MByte
	1280 x 1024	16,256,32k,64k	4MByte

4.10.8 Video Input Board V2.1a and older with the VPX3220

The 65554/555 Series integrated configuration reguires only a NTSC/PAL decoder VPX 3220A (from ITT) and standard DRAMs, without additional memory. The ITT decoder implements a 3 channel video multiplexer, which may be software controlled over the I2C bus.

To test the video input, you need to load WIN95 and the DIGITAL-LOGIC's demonstration program. Connect up to three cameras or other video sources (PAL or NTSC) to the video input connector and start the system. In the demo program you may select the signal type and the channels to display on the screen.

Resolutions:

65554	320 x 240 pixel	up to 30 images per second
65555	512 x 720 pixel	up to 30 images per second

The image may be overlayed or captured and stored into a file. To program this circuit, you need the C&T 65554 manual (to download from the C&T webpage) and the ITT PAL/NTSC decoder datasheet VPX3220A.

From C&T there are also some demo programs and driver examples in C++.

4.11 HiQ Video Multimedia Support

The 69000 uses independent multimedia capture and display systems on chip. The capture system places data in display memory (usually off screen) and the display system places the data in a window on the screen.
The capture system can receive data from the video portin the 422 YUV format. The YUV data are served from the VideoInputProcessor (VIP) type SAA7111A. The VIP converts the analog CVBS information, coming from a videocamera, into the YUV digital information.
The YUV input data can also be scaled down in the 69000 bevor storage in the display memory. Capture of input data may also be double buffered for smoothing and to prevent image tearing. To better support MPEG2 (DVD) video decompression, the 69000 includes a line buffer to directly support the native format of MPEG2 data of 720 pixels wide.

The capture engine also supports image mirroring and rotation for camera support. This feature is important for applications such as video teleconferencing because it allows the image movements to appear on the display as it actually occurs.

The display system can independently place YUV data from anywhere in the display memory into an on-screen window which can be any size and located at any pixel boundary (YUV data is converted to RGB „on-the-fly“). This is important for the 69000 since the video must be stored in the integrated 2MB frame buffer and thus optimized to require very little space. Interlanced and non-interlanced data are both supported in the capture and display system.

Display Modes Supported

The 69000 supports the modes which appear in the table below.

Resolution:	Color (bpp)	Refresh Rates (Hz)
640 x 480	8	60, 75, 85
640 x 480	16	60, 75, 85
640 x 480	24	60, 75, 85
800 x 600	8	60, 75, 85
800 x 600	16	60, 75, 85
800 x 600	24	60, 75, 85
1024 x 768	8	60, 75, 85
1024 x 768	16	60, 75, 85
1280 x 1024	8	60

4.11.1 HiQVideo Series Programming Examples

4.11.1.1 Introduction

This application note shows how the CHIPS HiQVideo??Series controllers can be used for video capture and playback. This document includes a description of the hardware configuration, a discussion of the functions, and actual programming examples.

4.11.1.2 Video Playback through PCI/VL Bus

The new generation of Chips and Technologies, Inc. Multimedia Accelerators (6555x) supports Color Space Conversion and Stretching (Zooming) in the back end with the chroma color key. The color space conversion functionality of the 6555x can be made available to video codecs by implementing the off-screen surface support in the DCI Provider (Windows 3.1 drivers). Only the playback feature of 6555x multimedia module is used to implement extended DCI functionality. This means the video input to the 6555x is kept in the frozen state (not grabbing) when DCI is running. For video playback, the CPU can write YUV, RGB15, and RGB16 data into the off-screen memory and fill the destination rectangle (where video need to be displayed on the visible screen) with the color key. Video can be zoomed up if the destination rectangle is bigger than the source rectangle in the off-screen buffer.

4.11.1.3 Video Capture and Playback Through Video Port

The new generation of CHIPS Multimedia Accelerators (6555x) can also capture live video from the video port into the off-screen memory and play it back with color space conversion onto a color keyed destination rectangle on the visible screen. Playback video can be zoomed up to fill the bigger destination rectangle while incoming video can be scaled down to fit into a smaller off-screen memory buffer or smaller destination rectangle. Zoomed video can be smoothed out with horizontal and vertical interpolation. Scaled down video can also be filtered out at input before capturing into the frame buffer. Input video can be cropped for the extra data which is usually associated with the NTSC or PAL video. The 6555x hardware can accommodate fast or slow capture applications through the CPU Bus by capturing the video frames in one of three methods: continuously, one frame at a time, or one every nth (n = 1-15) frame. Following diagram demonstrates the video capture.

VideoRect comes from the input video stream fed through the Video Port (VAFC / ZV Port) and comprises of one of the following sizes based on the input source.

NSTC:	640x480 60 fields / second (interlaced), Square Aspect Ratio (4:3).
	720x486 60 fields / second (interlaced), Non-square Aspect Ratio.
PAL:	768x576 50 fields / second (interlaced), Square Aspect Ratio (4:3).
	720x576 50 fields / second (interlaced), Non-square Aspect Ratio.
MPEG1:	320x240 30 frames / sec (non-interlaced), Square Aspect Ratio (4:3).
	352x288 30 frames / sec (non-interlaced), Non-square Aspect Ratio.
	Top-left of VideoRect is always at (0,0).

CropRect is defined relative to the **VideoRect**. **CropRect** is used to crop off some pixels from the top, left, right, or bottom to fit the image into a square pixel ratio or to drop some unwanted pixels. **CropRec**t is programmed using the acquisition window registers After cropping, the video is scaled down to fit into a smaller memory buffer or in a smaller display window. The scaled video is captured into off-screen video memory buffer or buffers (as in double buffer mode). There is a horizontal filter to reduce the sampling artifacts caused by input video scaling. Video in the capture buffer is displayed on top of the pixels which matches the color key and/or with a specified rectangular window.

4.11.1.4 ZoomUp

If client area of a window (**DispRect**) is larger than the capture buffer rectangle (**CaptRect**), the video can be zoomed up to fit into the DispRect.

4.11.1.5 Video Capture Using the Video Port

We need some additional functions to manage video capture through video port. Some of the initialization and exit code can be merged together with the playback code. Capture code should also include the previously described playback code.

4.11.2 How to enable video capture and playback module (Init)

This code should be executed before video starts flowing into the port.
1. Save and Set XRD0[4] = 1
2. Save and Set SAR04 = 0x2A; // To get wider (> 352) playback buffer width
Static USHORT XR60,XRD0,SAR04;

```
CaptureInit()

{
UCHAR XR_Index;
bVideoFlowingIn = 0; // assume video is not flowing into the port
XR_Index = ReadPortUshort(ulXrAddr); // Save XR Index
WritePortUchar(ulXrAddr,0xd0); // Read XRD0
xrD0 = ReadPortUshort(ulXrAddr); // Save XRD0
WritePortUshort(ulXrAddr,xrD0 | 0x7000);
// Enable video playback/Capture module
//
// Enable video port in 55x for ZV Port Style Video
//
WritePortUchar(ulXrAddr,0x60); // Read XR60
xr60 = ReadPortUshort(ulXrAddr); // Save XRD0
WritePortUshort(ulXrAddr,xr60 | 0x0300);
//
// Program 55x for playback of wider (> 352) video buffer.
//
WritePortUshort(ulXrAddr,0x044e); // Read SAR04
WritePortUchar(ulXrAddr,0x4f);
SAR04 = ReadPortUshort(ulXrAddr); // Save SAR04
WritePortUshort(ulXrAddr,(SAR04 & 0x00ff) | 0x2a00); // SAR04=2a
WritePortUchar(ulXrAddr,XR_Index); // Restore XR_Index
//
// Set video capture buffer address for both buffers.
//
u.d = osbMemAddress; // assign to a DWORD uinon to access bytes
WritePortUshort(ulMrAddr,((UINT)u.b[0] << 8) | MR_VIN_ADDR_1_L); //mr06
WritePortUshort(ulMrAddr,((UINT)u.b[1] << 8) | MR_VIN_ADDR_1_M); //mr07
WritePortUshort(ulMrAddr,((UINT)u.b[2] << 8) | MR_VIN_ADDR_1_H); //mr08
WritePortUshort(ulMrAddr,((UINT)u.b[0] << 8) | MR_VIN_ADDR_2_L); //mr09
WritePortUshort(ulMrAddr,((UINT)u.b[1] << 8) | MR_VIN_ADDR_2_M); //mr0a
WritePortUshort(ulMrAddr,((UINT)u.b[2] << 8) | MR_VIN_ADDR_2_H); //mr0b
WritePortUshort(ulMrAddr,((UINT)u.b[0] << 8) | MR_VDP_ADDR_1_L); //mr22
WritePortUshort(ulMrAddr,((UINT)u.b[1] << 8) | MR_VDP_ADDR_1_M); //mr23
WritePortUshort(ulMrAddr,((UINT)u.b[2] << 8) | MR_VDP_ADDR_1_H); //mr24
WritePortUshort(ulMrAddr,((UINT)u.b[0] << 8) | MR_VDP_ADDR_2_L); //mr25
WritePortUshort(ulMrAddr,((UINT)u.b[1] << 8) | MR_VDP_ADDR_2_M); //mr26
WritePortUshort(ulMrAddr,((UINT)u.b[2] << 8) | MR_VDP_ADDR_2_H); //mr27
//
// Set Aquisition rectangle to NULL (Left=-1, right=0) to avoid capturing of first
// frame. This is needed to latch the capture counter with the new address.
//
WritePortUshort(ulMrAddr,0xff0e); // program Left=-1
WritePortUshort(ulMrAddr,0xff0f);
WritePortUshort(ulMrAddr,0x0010); // program right=0
WritePortUshort(ulMrAddr,0x0011);
WritePortUshort(ulMrAddr,0x0012); // program top=0
WritePortUshort(ulMrAddr,0x0013);
WritePortUshort(ulMrAddr,0x0014); // program bottom=0
WritePortUshort(ulMrAddr,0x0015);
```

4.11.3 How to disable video playback and capture module (Exit)

1. Restore XRD0.
2. Restore SAR04.

```
UCHAR XR_Index;
XR_Index = ReadPortUshort(ulXrAddr); // Save XR Index
WritePortUshort(ulXrAddr,XRD0); // Restore XRD0
WritePortUshort(ulXrAddr,0x044e); // Read SAR04
WritePortUshortAddr,SAR04); // Restore SAR04
WritePortUchar(ulXrAddr,XR_Index); // Restore XR_Index
```

4.11.4 How to start video capture

```
// In 55x VGAs, capture counters are not updated with the new off-screen
// address until the next Input Video VSync. So, the first frame of the input
// video is captured at the old address left in the counters when we froze
// the video. This may cause the memory corruption. To avoid this problem we
// need to ignore the data of the first input video frame. We already set the
// acquisition window to NULL during initialization. Now all we have to do is to
// wait for the first couple of input Vsyncs then set the acquisition rectangle
// to proper values. Acquisition rectangle must not be set till video started
// flowing in (bVideoFlowingIn = 1). bVideoFlowingIn flag is set to 0 at
// initialization time.
// So let us perform the first frame ritual.
//
if(!bVideoFlowingIn)
{ // This is first time to start 550 video, see if video is flowing?
start_time = timeGetTime(); // 1 millisec precision
while(((timeGetTime() - start_time) < 200))
{ // wait for 200 milisec (33.3 ms for 30Hz video) and VSyncActivity
WritePortUchar(ulMrAddr, MR_VIN_CTRL_4);
if(ReadPortUshort(ulMrAddr) & (VIC4_VSYNC << 8))
{
bVideoFlowingIn = 1; // video start flowing
//
// Wait for Input VSync is over.
//
start_time = timeGetTime(); // 1 millisec precision
WritePortUchar(ulMrAddr, MR_VIN_CTRL_4);
while((ReadPortUshort(ulMrAddr) & (VIC4_VSYNC << 8)) &&
((timeGetTime() - start_time) < 200));
//
// Now wait for next VSync.
//
start_time = timeGetTime(); // 1 millisec precision
WritePortUchar(ulMrAddr, MR_VIN_CTRL_4);
while(!(ReadPortUshort(ulMrAddr) & (VIC4_VSYNC << 8)) &&
((timeGetTime() - start_time) < 200));
//
// Restore crop.right
//
SetCropRect((LPRECTL)&rCrop);
break;
}
}
} // FirstTime VideoFlowingIn
mr03 |= (VIC2_START_GRAB << 8); // unfreeze the video (start capturing)
WritePortUshort(ulMrAddr,mr03); // write new value
```

4.11.5 How to stop video capture

```
//---------------------------------------------------------------------------
// FreezeVideo() : Stops capturing the incoming video; whatever is in the
// frame buffer is being displayed.
//
// Enter:
// none
// Exit :
// Nothing
//---------------------------------------------------------------------------
void FreezeVideo()
{
int mr03;
DWORD start_time;
WritePortUchar(ulMrAddr, MR_VIN_CTRL_2);
mr03 = ReadPortUshort(ulMrAddr); // Read current value
if((mr03 & (VIC2_START_GRAB << 8)))
{ // video is running, h/w is grabbing video, wait for input VSync
mr03 &= ~(VIC2_START_GRAB << 8); // turn off the bit to freeze the video
//
// Sometimes if Video Input is not comming thru video port (ZV Port
// Disabled) then we will never get Video VSync (hanging problem). We must
// time out our wait for VSync. If we do not see VSync within 2 frames
// of input VSync (80 Miliseconds for 25Hz Video, worst case) we must get
// out of the waiting loop.
//
start_time = timeGetTime(); // 1 millisec precision
WritePortUchar(ulMrAddr, MR_VIN_CTRL_4);
while( !(ReadPortUshort(ulMrAddr) & (VIC4_VSYNC << 8)) &&
((timeGetTime() - start_time) < 200));
WritePortUshort(ulMrAddr, mr03); // freeze the video
start_time = timeGetTime(); // 1 millisec precision
WritePortUchar(ulMrAddr, MR_VIN_CTRL_4);
while((ReadPortUshort(ulMrAddr) & (VIC4_FRM_READY << 8)) &&
((timeGetTime() - start_time) < 200));
```

4.11.6 How to set input video color format

CHIPS 6555x supports three basic color formats which are YUV4:2:2, RG555 and RGB565. Each format is 16 bit per pixel. The 6555x also allows swapping of the UV positions within a 32 bit dword. The default sequence for YUV4:2:2 is Byte0=Y0, Byte1=U, Byte2=Y1, Byte3=V. The following code shows the input video format selection.

```
//-----------------------------------------------------------------------------
// SetVideoInputFormat() - sets Video Transfer Format bits
//-----------------------------------------------------------------------------
int ChipsVideoOverlay::SetVideoInputFormat(int iVideoFormat)
{
UINT i;
WritePortUchar(ulMrAddr,MR_VIN_CTRL_1); // read video display control reg1
i = ReadPortUshort(ulMrAddr);
i &= ~(VIC1_FORMAT << 8); // clear format bits (0 is YUV4:2:2)
switch(iVideoFormat)
{
case CMM_FMT_YUV_422:
// i |= (VIC1_YUV422 << 8); // 0 is YUV 4:2:2
break;
case CMM_FMT_RGB_555:
i |= (VIC1_RGB555 << 8);
break;
case CMM_FMT_RGB_565:
i |= (VIC1_RGB565 << 8);
break;
default:
return;
}
WritePortUshort(ulMrAddr,i); // write new format
}
```

4.11.7 How to set interlaced or non-interlaced video input

CHIPS 6555x supports interlaced or non-interlaced video sources. Usually, the NTSC/PAL video sources are interlaced and the hardware MPEG decoder generates non-interlaced video source. Following code selects video input type.

```
void SetVideoInputBits(BOOL interlaced)
{ // interlaced = 1 for interlaced video source
int mr02;
WritePortUchar(ulMrAddr, MR_VIN_CTRL_1);
mr02 = ReadPortUshort(ulMrAddr); // Read current value
mr02 &= ~(VIC1_NONINTERLACE << 8); // assume interlaced video
if(interlaced) mr02 |= (VIC1_NONINTERLACE << 8);
WritePortUshort(ulMrAddr, mr02); // write new value
```

4.11.8 How to enable/disable double buffer

CHIPS 6555x supports double buffering for the video capture and playback. Double buffering needs more memory but it minimizes the tearing effect generated by fast changing pictures. We assume that there is enough memory to accommodate both buffers and that the buffer address is programmed in (MR06, MR07, MR08, MR09, MR0A, MR0B). The following code sets/resets double buffering.

```
void SetDoubleBuffer(BOOL double_buffer)
{ // double_buffer = 1 to enable double buffer
int mr04,mr20;
WritePortUchar(ulMrAddr, MR_VIN_CTRL_3);
mr04 = ReadPortUshort(ulMrAddr); // Read current value
mr04 &= ~((VIC3_DB_VLOCK+VIC3_ENABLE_DB) << 8); // assume no double buffer
if(interlaced) mr04 |= ((VIC3_DB_VLOCK+VIC3_ENABLE_DB) << 8);
WritePortUshort(ulMrAddr, mr04); // write new value
//
// Enable double buffer for video playback which locked with the input VSync.
//
WritePortUchar(ulMrAddr, MR_VDP_CTRL_3);
mr20 = ReadPortUshort(ulMrAddr); // Read current value
mr20 &= ~((VDC3_DB_VLOVK+VDC3_DB_TRIGGER) << 8); // assume no double buffer
if(interlaced) mr20 |= ((VDC3_DB_VLOVK+VDC3_DB_TRIGGER) << 8);
WritePortUshort(ulMrAddr, mr20); // write new value
```

4.11.9 How to scale input video (before acquiring into frame buffer)

CHIPS 6555x can scale down the video before capturing into the off-screen buffer.

```
//-----------------------------------------------------------------------------
// SetVideoInputScale() : Sets video input scaling factors. Video input scaling
// factor depends on aquisition rectangle and frame buffer rectangle (source
// rectangle).
//
// Enter:
// wCrop = crop rectangle width
// hCrp = crop rectangle height
// wCap = Capture buffer width
// hCap = Capture buffer height
// Exit :
// Nothing
//-----------------------------------------------------------------------------
void SetVideoInputScale(int wCrop, int hCrop, int wCap, int hCap)
{
UINT mr03,scale_x,scale_y;
WritePortUchar(ulMrAddr, MR_VIN_CTRL_2);
mr03 = ReadPortUshort(ulMrAddr);
mr03 &= ~((VIC2_SCALE_X | VIC2_SCALE_Y) << 8); // assume no scaling
if(wCrop > wCap)
{ // horizontal input scaling needed
scale_x = (int)(((DWORD)wCap*VIN_SCALE_X_MAX) / (DWORD)wCrop);
WritePortUshort(ulMrAddr, (scale_x << 8) | MR_VIN_SCALE_X);
mr03 |= (VIC2_SCALE_X << 8); // enable input scaling
}
if(hCrop > hCap)
{ // vertical input scaling needed
scale_y = (int)(((DWORD)hCap*VIN_SCALE_Y_MAX) / (DWORD)hCrop);
WritePortUshort(ulMrAddr, (scale_y << 8) | MR_VIN_SCALE_Y);
mr03 |= (VIC2_SCALE_Y << 8); // enable input scaling
}
WritePortUshort(ulMrAddr, mr03); // set scale factors
```

4.11.10 How to crop input video (programming of acquisition rectangle)

Video acquisition rectangle is used to crop the unwanted video input data before the 6555x hardware scales it and grabs it into off-screen buffer. This is also used to crop vertical blank interval data (Closed Caption or Tele Text) from the NTSC video.

```
//-----------------------------------------------------------------------------
// SetCropRect() : Sets cropping rectrangle on input video recctangle.
//
// +----------------+
// | +----------+   |
// | |          |   |
// | | CropRect |   |
// | |          |   |
// | +----------+   |
// | Input Video    |
// +----------------+
//
// Enter:
// lpRect Crop Rectangle withing Input Video rectangle (NTSC/PAL dependent)
// rCrop - local copy of Cropping Rectangle
// bVideoFlowingIn = 0 if video is not flowing into the port, 1 normally.
// Exit :
// Nothing
//-----------------------------------------------------------------------------
void SetCropRect(LPRECTL lpRect)
{
UINT mr0e,mr0f,mr10,mr11,mr12,mr13,mr14,mr15;
union WORD16 u;
if(&rCrop != lpRect) rCrop = *lpRect; // copy crop rectangle into our area
if(!bVideoFlowingIn) return;
// Use NULL Rectangle done by static initialization
u.w = (USHORT)((int)rCrop.left);
mr0e = ((UINT)u.b[0] << 8) + MR_VIN_AQW_XL_L;
mr0f = ((UINT)u.b[1] << 8) + MR_VIN_AQW_XL_H;
u.w = (USHORT)((int)rCrop.right -1);
mr10 = ((UINT)u.b[0] << 8) + MR_VIN_AQW_XR_L;
mr11 = ((UINT)u.b[1] << 8) + MR_VIN_AQW_XR_H;
u.w = (USHORT)((int)rCrop.top);
mr12 = ((UINT)u.b[0] << 8) + MR_VIN_AQW_YT_L;
mr13 = ((UINT)u.b[1] << 8) + MR_VIN_AQW_YT_H;
u.w = (USHORT)((int)rCrop.bottom -1);
mr14 = ((UINT)u.b[0] << 8) + MR_VIN_AQW_YB_L;
mr15 = ((UINT)u.b[1] << 8) + MR_VIN_AQW_YB_H;
WritePortUshort(ulMrAddr,mr0e); // program Left
WritePortUshort(ulMrAddr,mr0f);
WritePortUshort(ulMrAddr,mr10); // program right
WritePortUshort(ulMrAddr,mr11);
WritePortUshort(ulMrAddr,mr12); // program top
WritePortUshort(ulMrAddr,mr13);
WritePortUshort(ulMrAddr,mr14); // program bottom
WritePortUshort(ulMrAddr,mr15);
```

Definition of CHIPSMM.H

```
/*************************************************************************
* Description: Hardware register definitiona file for 6555x *
* Copyright (C) Chips and Technologies, Inc. 1995 *
*************************************************************************/
#define WritePortUchar(p,v) outp((USHORT)p,v)
#define WritePortUshort(p,v) outpw((USHORT)p,v)
#define WritePortUlong(p,v) outpd((USHORT)p,v)
#define ReadPortUchar(p) inp((USHORT)p)
#define ReadPortUshort(p) inpw((USHORT)p)
#define ReadPortUlong(p) inpd((USHORT)p)
//-----------------------------------------------------------------------
// Chips multimedia register description for 6555x registers.
// Any chages here must also be made in CHIPSMMH.INC
//-----------------------------------------------------------------------
#define ADDR_FR 0x03d0 // C&T Flat Panel Register address port
#define DATA_FR 0x03d1 // C&T Flat Panel Register data port
#define ADDR_MR 0x03d2 // C&T Multimedia Register address port
#define DATA_MR 0x03d3 // C&T Multimedia Register data port
#define ADDR_EXTR 0x03d6 // C&T XR Address
#define DATA_EXTR 0x03d7 // C&T XR Data
#define MR_CAPS_REG_1 0x00 // Multimedia capabilities reg 1
#define MR_CAPS_REG_2 0x01 // Multimedia capabilities reg 2
#define MR_VIN_CTRL_1 0x02 // Video Input Control Reg 1
#define MR_VIN_CTRL_2 0x03 // Video Input Control Reg 2
#define MR_VIN_CTRL_3 0x04 // Video Input Control Reg 3
#define MR_VIN_CTRL_4 0x05 // Video Input Control Reg 4(stat reg)
#define MR_VIN_ADDR_1_L 0x06 // Video Input Address Pointer 1 (low)
#define MR_VIN_ADDR_1_M 0x07 // Video Input Address Pointer 1 (mid)
#define MR_VIN_ADDR_1_H 0x08 // Video Input Address Pointer 1 (high)
#define MR_VIN_ADDR_2_L 0x09 // Video Input Address Pointer 2 (low)
#define MR_VIN_ADDR_2_M 0x0A // Video Input Address Pointer 2 (mid)
#define MR_VIN_ADDR_2_H 0x0B // Video Input Address Pointer 2 (high)
#define MR_VIN_PITCH_QD 0x0C // Pitch of Video Input buff in quad
// words (8 bytes = 1QD)
#define MR_VIN_AQW_XL_L 0x0E // Aquisition Window X-Left low
#define MR_VIN_AQW_XL_H 0x0F // Aquisition Window X-Left high
#define MR_VIN_AQW_XR_L 0x10 // Aquisition Window X-Right low
#define MR_VIN_AQW_XR_H 0x11 // Aquisition Window X-Right high
#define MR_VIN_AQW_YT_L 0x12 // Aquisition Window Y-Top low
#define MR_VIN_AQW_YT_H 0x13 // Aquisition Window Y-Top high
#define MR_VIN_AQW_YB_L 0x14 // Aquisition Window Y-Bottom low
#define MR_VIN_AQW_YB_H 0x15 // Aquisition Window Y-Bottom high
#define MR_VIN_SCALE_X 0x16 // Video Input Horizontal scale factor
#define MR_VIN_SCALE_Y 0x17 // Video Input Vertical scale factor
#define MR_VIN_FRMCOUNT 0x18 // Frame Count for Nth Frame capturing
//-----------------------------------------------------------------------
// Video Display Registers:
//-----------------------------------------------------------------------
#define MR_VDP_CTRL_1 0x1E // Video Display Control Reg 1
#define MR_VDP_CTRL_2 0x1F // Video Display Control Reg 2
#define MR_VDP_CTRL_3 0x20 // Video Display Control Reg 3
#define MR_VDP_CTRL_4 0x21 // Video Display Control Reg 4 (status)
#define MR_VDP_ADDR_1_L 0x22 // Video Display Addr Pointer 1 (low)
#define MR_VDP_ADDR_1_M 0x23 // Video Display Addr Pointer 1 (mid)
#define MR_VDP_ADDR_1_H 0x24 // Video Display Addr Pointer 1 (high)
#define MR_VDP_ADDR_2_L 0x25 // Video Display Addr Pointer 2 (low)
#define MR_VDP_ADDR_2_M 0x26 // Video Display Addr Pointer 2 (mid)
#define MR_VDP_ADDR_2_H 0x27 // Video Display Addr Pointer 2 (high)
```

```
#define MR_VDP_PITCH_QD 0x28 // Pitch of Video Display Window in
// quad words (8 bytes = 1QD)
#define MR_VDP_WIN_XL_L 0x2A // Display Window X-Left low
#define MR_VDP_WIN_XL_H 0x2B // Display Window X-Left high
#define MR_VDP_WIN_XR_L 0x2C // Display Window X-Right low
#define MR_VDP_WIN_XR_H 0x2D // Display Window X-Right high
#define MR_VDP_WIN_YT_L 0x2E // Display Window Y-Top low
#define MR_VDP_WIN_YT_H 0x2F // Display Window Y-Top high
#define MR_VDP_WIN_YB_L 0x30 // Display Window Y-Bottom low
#define MR_VDP_WIN_YB_H 0x31 // Display Window Y-Bottom high
#define MR_VDP_ZOOM_X 0x32 // Video Display Horizontal Zoom factor
#define MR_VDP_ZOOM_Y 0x33 // Video Display Vertical Zoom factor
//-----------------------------------------------------------------------
// Color key registers
//-----------------------------------------------------------------------
#define MR_VDP_CKEY_CTRL 0x3C // Video Color Key Control
#define MR_VDP_CKEY_0 0x3F //sw Graphics Color Key Reg 0 (blue)
#define MR_VDP_CKEY_1 0x3E // Graphics Color Key Reg 1 (green)
#define MR_VDP_CKEY_2 0x3D //sw Graphics Color Key Reg 2 (red)
#define MR_VDP_CKEY_M0 0x42 //sw Graphics Color Key Mask Reg0(blue)
#define MR_VDP_CKEY_M1 0x41 // Graphics Color Key Mask Reg1 (green)
#define MR_VDP_CKEY_M2 0x40 //sw Graphics Color Key Mask Reg2 (red)
#define MR_CRT_SCAN_LO 0x43 // Current CRTC Refresh Scanline Line
// Read Counter lo 8 bits
#define MR_CRT_SCAN_HI 0x44 // Current CRTC Refresh Scanline Line
// Read Counter hi 4 bits
//-----------------------------------------------------------------------
// Multimedia capabilities register_1 definitions (MR00):
//-----------------------------------------------------------------------
#define MCAPS_PLAYBACK 0x01 // Play back available
#define MCAPS_CAPTURE 0x02 // Capture available
//-----------------------------------------------------------------------
// Bit definition of Video Input Control Register1 (MR_VIN_CTRL_1)
//-----------------------------------------------------------------------
#define VIC1_NONINTERLACE 0x01 // Interlaced video input
#define VIC1_GAMEFORMAT 0x02 // Game format (duplicate field) video
#define VIC1_YUV422 0x00 // Video Input is YUV
#define VIC1_RGB565 0x04 // RGB16 video input (0 is YUV)
#define VIC1_RGB555 0x0C // RGB15 video input
#define VIC1_FORMAT 0x0E // all format bits
#define VIC1_HSYNC_HI 0x10 // H-Sync Polarity : Hi asserted
#define VIC1_VSYNC_HI 0x20 // V-Sync Polarity : Hi asserted
#define VIC1_FLD_DT_INV 0x40 // Field detect polarity inverted
#define VIC1_FLD_DT_LDE 0x80 // Field detect method leading edge
//-----------------------------------------------------------------------
// Bit definition of Video Input Control Register2 (MR_VIN_CTRL_2)
//-----------------------------------------------------------------------
#define VIC2_START_GRAB 0x01 // 1:start grab, 0:stop grab
#define VIC2_SINGLE 0x02 // 1:single frame, 0:continuous
#define VIC2_FIELD_GRAB 0x04 // 1:field grab, 0:frame grab
#define VIC2_ODD_FIELD 0x08 // 1:odd field grab, 0:even filed grab
#define VIC2_SCALE_X 0x10 // 1:enable x_scaling, 0:full screen
#define VIC2_SCALE_Y 0x20 // 1:enable y_scaling, 0:full screen
#define VIC2_YSCALE_ES 0x40 // 1:y-scale even spaced, 0:normal
#define VIC2_YSCALE_OW 0x80 // y-scale overwrite, 0:as per prev bit
//-----------------------------------------------------------------------
// Bit definition of Video Input Control Register3 (MR_VIN_CTRL_3)
//-----------------------------------------------------------------------
#define VIC3_X_MIRRORED 0x01 // capture direction, 1:right to left,
// 0: left to right
```

```
#define VIC3_Y_FLIPPED 0x02 // capture direction, 1:bottom to top,
// 0: top to bottom
#define VIC3_HFILTER 0x04 // 1:enable horizontal filter at input,
// 0:no h filter
#define VIC3_DB_VLOCK 0x08 // 1:DoubleBuffer Vsync locked,
// 0:DoubleBuffer CPU forced
#define VIC3_ENABLE_DB 0x10 // 1:Enable DoubleBuffer,
// 0:No DoubleBuffer
#define VIC3_PTR1_INUSE 0x20 // 1:PTR 1 in use for DoubleBuffer,
// 0:PTR 0 in use for DoubleBuffer
#define VIC3_CAPTURE_NF 0x80 // 1:Capture Nth Frame/Field,
// 0:Capture single frame
//-------------------------------------------------------------------------
// Bit definition of Video Input Status Register (MR_VIN_CTRL_4)
//-------------------------------------------------------------------------
#define VIC4_FRM_READY 0x01 // 1:Frame is ready for grab by CPU
// (synced with VSync)
#define VIC4_VSYNC 0x08 // VSync after polarity correction
// (read only)
#define VIC4_PQE_PIXEL 0x10 // 1:Pixel Qualifier as valid pixel
// 0:Pixel Qualifier as Blank signal
#define VIC4_PQP_INV 0x20 // 1:Pixel Qualifier polarity inverted,
// 0:Pixel Qualifier normal
#define VIC4_SWAP_UV 0x40 // 1:Swap U & V,
// 0:UV Normal sequence
#define VIC4_HY_LUV 0x80 // 1:Y on high and UV on low pins(VESA)
// 0:UV on high and Y on low pins
//-------------------------------------------------------------------------
// Bit definition of Video Display Control Register1 (MR_VDP_CTRL_1)
//-------------------------------------------------------------------------
#define VDC1_X_MIRRORED 0x01 // 1:mirrored (right to left),
// 0:normal (left to right)
#define VDC1_Y_FLIPPED 0x02 // 1:Flipped (bottom to top),
// 0:normal (top to bottom)
#define VDC1_ZOOM_X 0x04 // 1:enable x_zoom (zoom based on reg),
// 0:normal
#define VDC1_ZOOM_Y 0x08 // 1:enable y_zoom (zoom based on reg),
// 0:normal
#define VDC1_INTERLACE 0x10 // 1:VGA Mode is interlaced,
// 0:non-interlaced mode
//-------------------------------------------------------------------------
// Bit definition of Video Display Control Register2 (MR_VDP_CTRL_2)
//-------------------------------------------------------------------------
#define VDC2_YUV422 0x00 // Video Buf is YUV4:2:2
#define VDC2_UV_SWAP 0x01 // Video Buf is YUV4:2:2 with UV Swap
#define VDC2_SIGNED_UV 0x02 // Video Buf is YUV4:2:2 with Signed UV
#define VDC2_YUV422_UVS 0x01 // Video Buf is YUV4:2:2 with UV Swap
#define VDC2_YUV422_SUV 0x02 // Video Buf is YUV4:2:2 with Signed UV
#define VDC2_YUV422_UV 0x03 // Video Buf is YUV4:2:2 Signed UV&Sawp
#define VDC2_RGB555 0x09 // Video Buffer is RGB15 (5-5-5)
#define VDC2_RGB565 0x08 // Video Buffer is RGB16 (5-6-5)
#define VDC2_FORMAT 0x1F // All format bits
#define VDC2_H_INTERPOL 0x20 // Enable Horizontal Interpolation
#define VDC2_VI_RUNAVRG 0x40 // Vertical Interpolation is done as
// running average method
#define VDC2_V_INTERPOL 0x80 // Enable Vertical Interpolation
//-------------------------------------------------------------------------
// Bit definition of Video Display Control Register3 (MR_VDP_CTRL_3)
//-------------------------------------------------------------------------
#define VDC3_DB_TRIGGER 0x08 // Display new pointer on next VSync
```

```
#define VDC3_DB_CPU_PTR 0x04 // 1:Dbl buf src is buf ptr set by CPU
// 0:Dbl buf src is Input Aqisition's
// last frame
#define VDC3_DB_PTR2 0x10 // 1:CPU buffer is pointer 2
// 0:CPU buffer is pointer 1
#define VDC3_DB_VLOVK 0x20 // 1:Double buffer is VSync locked
// 0:Double buffer is unlocked
//-------------------------------------------------------------------------
// Bit definition of Video Display Status Register4 (MR_VDP_CTRL_4)
//-------------------------------------------------------------------------
#define VDC4_DB_PENDING 0x01 // 1:hasn't displayed CPU set buffer
// 0:CPU Set buffer is displayed or in
// process of being displayed
#define VDC4_DB_USEPTR2 0x02 // 1:PTR2 is being displayed
// 0:PTR1 is being displayed
//-------------------------------------------------------------------------
// Bit definition of Video Color Key Control Register (MR_VDP_CKEY_CTRL)
//-------------------------------------------------------------------------
#define VDC_EV_OVERLAY 0x01 // 1:Enable video overlay
// 0:Display graphics only
#define VDC_EV_COLOR_KEY 0x02 // 1:Enable video display using clr key
// 0:Color Key Disabled
#define VDC_EV_XY_RECT 0x04 // 1:Enable video display in Rect Rgn
// 0:Video Display in Rect Rgn disabled
#define VDC_ENABLE_VAFC 0x08 // 1:Enable external VAFC (like 545)
// for color key only
// 0:Our own video play back
#define VDC_VAFC_18 0x10 // 1:18 bit external VAFC
// 0:16 bit external VAFC
#define VDC_BIT_15_KEY 0x40 // 1:in 16BPP modes MSB is routed thru
// Blue0 for color key
// 0:normal color key
#define VDC_BIT_0_KEY 0x80 // 1:enable blue0 clr key for 16/24BP
// 0:normal color key for 16/24BPP mode
#define VIN_SCALE_X_MAX 0x100 // max value of x_scale reg (8 bit reg)
#define VIN_SCALE_Y_MAX 0x100 // max value of y_scale reg (8 bit reg)
//#define VDP_ZOOM_X_MAX 0x100 // max value of x_zoom reg (ES1 100h)
//#define VDP_ZOOM_Y_MAX 0x100 // max value of y_zoom reg (ES1 100h)
#define VDP_ZOOM_X_MAX 0x40 // max value of x_zoom reg (ES0 40h)
#define VDP_ZOOM_Y_MAX 0x40 // max value of y_zoom reg (ES0 40h)
/*
```

4.11.11 Video Input board V2.2 and newer with the SAA7111 VIP

The 65554/555 Series integrated configuration reguires only a NTSC/PAL decoder VPX 3220A (from ITT) and standard DRAMs, without additional memory. The ITT decoder implements a 3 channel video multi-plexer, which may be software controlled over the I2C bus.

4.11.11.1 Features of the SAA7111A VideoInput Processor

- Four analog inputs, internal analog source selectors, e.g. 4 CVBS or 2 Y/C or (1 Y/C and 2 CVBS)
- Two analog preprocessing channels
- Fully programmable static gain for the main channels or automatic gain control for the selected CVBS or Y/C channel
- Switchable white peak control
- Two built-in analog anti-aliasing filters
- Two 8-bit video CMOS analog-to-digital converters
- On-chip clock generator
- Line-locked system clock frequencies
- Digital PLL for horizontal-sync processing and clock generation
- Requires only one crystal (24.576 MHz) for all standards
- Horizontal and vertical sync detection
- Automatic detection of 50 and 60 Hz field frequency, and automatic switching between PAL and NTSC standards
- Luminance and chrominance signal processing for PAL BGHI, PAL N, PAL M, NTSC M, NTSC N, NTSC 4.43, SECAM
- User programmable luminance peaking or aperture correction
- Cross-colour reduction for NTSC by chrominance comb filtering
- PAL delay line for correcting PAL phase errors
- Real time status information output (RTCO)
- Brightness Contrast Saturation (BCS) control on-chip
- The YUV (CCIR-601) bus supports a data rate of:
    - 864 ??fH = 13.5 MHz for 625 line sources
    - 858 ??fH = 13.5 MHz for 525 line sources.
- Data output streams for 16, 12 or 8-bit width with the following formats:
    – YUV 4 :1 :1 (12-bit)
    – YUV 4 :2 :2 (16-bit) = used on the product
    – YUV 4 :2 :2 (CCIR-656) (8-bit)
    – RGB (5, 6, and 5) (16-bit) with dither
    – RGB (8, 8, and 8) (24-bit) with special application.
- Odd/even field identification by a non interlace CVBS input signal
- Fix level for RGB output format during horizontal blanking
- 720 active samples per line on the YUV bus
- One user programmable general purpose switch on an output pin
- Built-in line-21 text slicer
- A 27 MHz Vertical Blanking Interval (VBI) data bypass programmable by I 2 C-bus for INTERCAST applications
- Power-on control
- Two via I 2 C-bus switchable outputs for the digitized CVBS or Y/C input signals AD1 (7 to 0) and AD2 (7 to 0)
- Chip enable function (reset for the clock generator and power save mode up from chip version 3)
- Compatible with memory-based features (line-locked clock)
- Boundary scan test circuit complies with the ‘IEEE Std. 1149.1??1990’ (ID-Code = 0 F111 02 B)
- I2C-bus controlled (full read-back ability by an external controller)
- Low power (0.5 W), low voltage (3.3 V), small package (LQFP64)
- 5 V tolerant digital I/O ports.

4.11.11.2 Operation of the SAA7111A VideoInput Processor

The SECAM-processing contains the following blocks:

Baseband 'bell' filters to reconstruct the amplitude and phase equalized 0 and 90??FM-signals

Phase demodulator and differentiator (FM-demodulation)

Pe-emphasis filter to compensate the pre-emphasised input signal, including frequency offset compensation (DB or DR white carrier values are subtracted from the signal, controlled by the SECAM-switch signal).
The burst processing block provides the feedback loop of the chroma PLL and contains;

Burst gate accumulator

Colour identification and killer

Comparison nominal/actual burst amplitude (PAL/NTSC standards only)

Loop filter chrominance gain control (PAL/NTSC standards only)

Loop filter chrominance PLL (only active for PAL/NTSC standards)

PAL/SECAM sequence detection, H/2-switch generation

Increment generation for DTO1 with divider to generate stable subcarrier for non-standard signals.

The chrominance comb filter block eliminates crosstalk between the chrominance channels in accordance with the

PAL standard requirements. For NTSC colour standards the chrominance comb filter can be used to eliminate crosstalk from luminance to chrominance (cross-colour) for vertical structures. The comb filter can be switched off if desired. The embedded line delay is also used for SECAM recombination (cross-over switches).
The resulting signals are fed to the variable Y-delay compensation, RGB matrix, dithering circuit and output interface, which contains the VPO output formatter and the output control logic.

Luminance processing
The 8-bit luminance signal, a digital CVBS format or a luminance format (S-VHS, HI8), is fed through a switchable prefilter. High frequency components are emphasized to compensate for loss. The following chrominance trap filter (f0 = 4.43 or 3.58 MHz centre frequency selectable) eliminates most of the colour carrier signal, therefore, it must be bypassed for S-video (S-VHS and HI8) signals. The high frequency components of the luminance signal can be peaked (control for sharpness improvement via I2C-bus) in two band-pass filters with selectable transfer characteristic. This signal is then added to the original (unpeaked) signal. A switchable amplifier achieves common DC amplification, because the DC gains are different in both chrominance trap modes. The improved luminance signal is fed to the BCS control located in the chrominance processing block.

RGB matrix
Y, Cr and Cb data are converted after interpolation into RGB data in accordance with CCIR-601 recommendations. The realized matrix equations consider the digital quantization:
R = Y + 1.371 Cr
G = Y 0.336 Cb 0.698 Cr
B = Y + 1.732 Cb.
After dithering (noise shaping) the RGB data is fed to the output interface within the VPO-bus output formatter.

VBI-data bypass
For a 27 MHz VBI-data bypass the offset binary CVBS signal is upsampled behind the ADCs. Upsampling of the CVBS signal from 13.5 to 27 MHz is possible, because the ADCs deliver high performance at 13.5 MHz sample clock. Suppressing of the back folded CVBS frequency components after upsampling is achieved by an interpolation filter. The TUF block on the digital top level performs the upsampling and interpolation for the bypassed CVBS signal.

VPO-bus (digital outputs)
The 16-bit VPO-bus transfers digital data from the output interfaces to a feature box or a field memory, a digital colour space converter (SAA7192 DCSC), a video enhancement and digital-to-analog processor (SAA7165 VEDA2) or a colour graphics board (Targa-format) as a graphical user interface.

5 DESCRIPTION OF THE CONNECTORS

Flat cable

- 44pin IDE is: IDT Terminal for Dual Row (2.00mm grid) and 1.00mm flat cable
- All others are: IDT Terminal for Dual Row 0.1" (2.54mm grid) and 1.27mm flat cable

Connector	Texture	Remarks
J01	FAN CPU	2 Pin
J05	LCD 1 (digital 36 Bit)	34 Pin
J06	CRT MONITOR DSub	15 Pin
J11	FLOPPY SMALL 26pin (MICROFLOPPY, not assembled)	26 Pin
J17	COM2	10 Pin
J18	LPT1	26 Pin
J21	FLOPPY NORMAL 34pin	34 Pin
J22	COM1 D-SUB	9 Pin
J23	E-IDE PRIMARY PORT SMALL 44pin (not assembled)	44 Pin
J25	E-IDE PRIMARY PORT NORMAL 40pin	40 Pin
J28	Battery	6 Pin
J31	UTILITY	14 Pin
J32	MOUSE (PS2)	6 Pin
J34/35	PC104-Bus	104 Pin
J36	Slot ISA-Bus	96 Pin
J38	SCSI 2	50 Pin
J40	ETHERNET 10 BASE – 2	2 Pin
J44	POWER +5V, GND, +12V	3 Pin
J56	LCD 2 (optional CRT signals for stackthrough)	8 Pin
J58	Temperature sensor	2 Pin
J58	NTC 100k (TEMPERATURE CONTROL)	2 Pin
J61	KEYBOARD (PS/2)	6 Pin
J62	Video Input	6 Pin
J64	ETHERNET 10 BASE – T	8 Pin
J65	PC104+ Bus	120 Pin
J70	Alternative 33Mhz crystal for AD1816 chip	3 Pin
J71	Sound Line In	3 Pin
J74	COM1	10 Pin
J90	Sound AUX In	2 Pin
J91	COM1 RS422/485	4 Pin
J93	COM2 RS422/485	4 Pin
J95	AUI	8 Pin
J97	USB (not supported)	6 Pin
J98	LAN BSE LED	2 Pin
J99	IDE HDD LED	2 Pin
J102	POWER LED	2 Pin
M1	BIG SIMM 1 (LOW)	72 Pin
M2	BIG SIMM 2 (HIGH)	72 Pin
U75	Flashdisk Socket for M-Systems DOC2000 module	32 Pin

J44 Power supply connector

Pin	Signal
Pin 1	VCC Logic, CPU
Pin 2	+12V for LCD and sound (ESS1869)
Pin 3	Ground

J22 = COM1 serial port connector, new since V2.2 (J74 optionally for stackthrough)

Channel:		Header onboard	D-SUB connector	Signal
COM	1:		Pin 1	= DCD
J22			Pin 6	= DSR
			Pin 2	= RxD
			Pin 7	= RTS
			Pin 3	= TxD
			Pin 8	= CTS
			Pin 4	= DTR
			Pin 9	= RI
			Pin 5	= GND

J17 = COM2 serial port connector

Channel:		Header onboard	D-SUB connector	Signal
COM	2:	Pin 1	Pin 1	= DCD
J17		Pin 2	Pin 6	= DSR
		Pin 3	Pin 2	= RxD (RS485-A) *
		Pin 4	Pin 7	= RTS
		Pin 5	Pin 3	= TxD (RS485-B) *
		Pin 6	Pin 8	= CTS
		Pin 7	Pin 4	= DTR
		Pin 8	Pin 9	= RI
		Pin 9	Pin 5	= GND
		Pin 10		= NC

* Until version V2.1, the RS485 option is an assembling option. In this case, these signals are available at the place of RXD and TXD of COM2.

J91 COM1 RS422/485 (4wire), new since V2.2

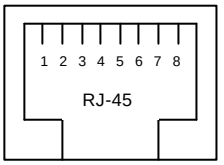
Pin	Signal
Pin 1	TX+
Pin 2	TX-
Pin 3	RX+
Pin 4	RX-

J93 COM2 RS422/485 (4wire), new since V2.2

Pin	Signal
Pin 1	TX+
Pin 2	TX-
Pin 3	RX+
Pin 4	RX-

J64 Ethernet Twisted Pair interface 10/100Mhz, (assembling option)

Pin J64 *	Signal	RJ-45 Pin	Signal
Pin 1	= TX+	Pin 1	= TX+
Pin 2	= TX-	Pin 2	= TX-
Pin 3	= RX+	Pin 3	= RX+
Pin 4	= RX-	Pin 6	= RX-
		Pin 4,5,7,8	pull down with 75ohms



* This signals are ready to connect directly to a RJ-45 connector.

J23 Optionally assembled IDE interface connector 44 pins RM2.00mm on rear side

Pin	Signal	Pin	Signal
Pin 1	= Reset (active low)	Pin 2	= GND
Pin 3	= D7	Pin 4	= D8
Pin 5	= D6	Pin 6	= D9
Pin 7	= D5	Pin 8	= D10
Pin 9	= D4	Pin 10	= D11
Pin 11	= D3	Pin 12	= D12
Pin 13	= D2	Pin 14	= D13
Pin 15	= D1	Pin 16	= D14
Pin 17	= D0	Pin 18	= D15
Pin 19	= GND	Pin 20	= NC (keypin)
Pin 21	= DRQ0	Pin 22	= GND
Pin 23	= IOW (active low)	Pin 24	= GND
Pin 25	= IOR (active low)	Pin 26	= GND
Pin 27	= IORD4	Pin 28	= VCC pullup
Pin 29	= DACK0	Pin 30	= GND
Pin 31	= IRQ14	Pin 32	= IOCS16 (active low)
Pin 33	= ADR1	Pin 34	= NC
Pin 35	= ADR0	Pin 36	= ADR2
Pin 37	= CS0 (active low)	Pin 38	= CS1 (active low)
Pin 39	= LED (active low)	Pin 40	= GND
Pin 41	= VCC Logic	Pin 42	= VCC Motor
Pin 43	= GND	Pin 44	= NC

J25 IDE interface connector – AT- IDE 3,5" 40 pins RM2.54

Pin	Signal	Pin	Signal
Pin 1	= Reset (active low)	Pin 2	= N.C.
Pin 3	= D7	Pin 4	= D8
Pin 5	= D6	Pin 6	= D9
Pin 7	= D5	Pin 8	= D10
Pin 9	= D4	Pin 10	= D11
Pin 11	= D3	Pin 12	= D12
Pin 13	= D2	Pin 14	= D13
Pin 15	= D1	Pin 16	= D14
Pin 17	= D0	Pin 18	= D15
Pin 19	= GND	Pin 20	= N.C. (keypin)
Pin 21	= N.C.	Pin 22	= GND
Pin 23	= IOW (active low)	Pin 24	= GND
Pin 25	= IOR (active low)	Pin 26	= GND
Pin 27	= NC	Pin 28	= ALE / Master-Slave (not used)
Pin 29	= NC	Pin 30	= GND
Pin 31	= IRQ14	Pin 32	= IOCS16 (active low)
Pin 33	= ADR1	Pin 34	= N.C.
Pin 35	= ADR0	Pin 36	= ADR2
Pin 37	= CS0 (active low)	Pin 38	= CS1 (active low)
Pin 39	= LED (active low)	Pin 40	= GND

J21 Floppy disk interface connector for 5,25" and 3,5" FD (34 pins header)

Pin	Signal	Pin	Signal
Pin 1,	= GND	Pin 2	= RPM
Pin 3	= GND	Pin 4	= NC
Pin 5	= GND	Pin 6	= NC
Pin 7	= GND	Pin 8	= INDEX
Pin 9	= GND	Pin 10	= Motor on device 0
Pin 11	= GND	Pin 12	= Drive select 1
Pin 13	= GND	Pin 14	= Drive select 0
Pin 15	= GND	Pin 16	= Motor on device 1
Pin 17	= GND	Pin 18	= Head direction
Pin 19	= GND	Pin 20	= Step
Pin 21	= GND	Pin 22	= Write data
Pin 23	= GND	Pin 24	= Write gate
Pin 25	= GND	Pin 26	= Track 00
Pin 27	= GND	Pin 28	= Write protection
Pin 29	= GND	Pin 30	= Read data
Pin 31	= GND	Pin 32	= Head selection 0/1
Pin 33	= GND	Pin 34	= Disk change signal

J11 Optionally assembled on the rear side for micro floppy 3,5" (26 pins FCC-header

Pin	Signal
Pin 1	= VCC
Pin 2	= Index
Pin 3	= VCC
Pin 4	= Drive select
Pin 5	= VCC
Pin 6	= Disk change signal
Pin 7	= nc
Pin 8	= nc
Pin 9	= nc
Pin 10	= Motor on
Pin 11	= nc
Pin 12	= Dir
Pin 13	= nc
Pin 14	= Step
Pin 15	= GND
Pin 16	= Write data
Pin 17	= GND
Pin 18	= Write gate
Pin 19	= GND
Pin 20	= Track 00
Pin 21	= GND
Pin 22	= Write protect
Pin 23	= GND
Pin 24	= Read data
Pin 25	= GND
Pin 26	= Head select

J18 Printerport connector (LPT1)

The printer connector provides an interface for 8 bit centronics printers.

Since V1.2

Header onboard	D-SUB connector on the cable	Signal
Pin 1	Pin 1	= Strobe
Pin 3	Pin 2	= Data 0
Pin 5	Pin 3	= Data 1
Pin 7	Pin 4	= Data 2
Pin 9	Pin 5	= Data 3
Pin 11	Pin 6	= Data 4
Pin 13	Pin 7	= Data 5
Pin 15	Pin 8	= Data 6
Pin 17	Pin 9	= Data 7
Pin 19	Pin 10	= Acknowledge
Pin 21	Pin 11	= Busy
Pin 23	Pin 12	= Paper end
Pin 25	Pin 13	= Select
Pin 2	Pin 14	= Autofeed
Pin 4	Pin 15	= Error
Pin 6	Pin 16	= Init printer
Pin 8	Pin 17	= Shift in (SI)
Pin 10,12,14,16,18	Pin 18 – 22	= Left open
Pin 20,22,24	Pin 23 – 25	= Ground

J61 PS/2 – keyboard connector

The keyboard connector, is a 6pin PS/2 connector that provides an interface for PS/2-keyboards.

J32 Pin	Keyboard Signal
Pin 1	= Keyboard Data
Pin 2	= GND
Pin 3	= GND
Pin 4	= VCC , + 5 Volt
Pin 5	= Keyboard Clock
Pin 6	= GND

J6 VGA-CRT connector (HiDens DSUB 15pin)

Pin	Signal
Pin 1	Red
Pin 2	Green
Pin 3	Blue
Pin 5	GND
Pin 6	GND
Pin 7	GND
Pin 8	GND
Pin 10	GND
Pin 13	H-Synch
Pin 14	V-Synch

J5 VGA-LCD 50pin RM2.00mm connector

Pin	Signal	Function
Pin 1	M/FPM	M-Clock
Pin 2	FLM	Frame
Pin 3	VBACKLSAFE	12V/1A for Backlight
Pin 4	LP	Line pulse
Pin 5	VCC for LCD	5V or 3.3V (selected by J54)
Pin 6	GND	0V
Pin 7	VEESAFE	5V / 1A for VEE Generator
Pin 8	SHFCLK	Shift clock
Pin 9	VDDSAFE	5V or +12V/1A for VDD-LCD (selected by J55)
Pin 10	P0	Data 0
Pin 11	P1	Data 1
Pin 12	P2	Data 2
Pin 13	P3	Data 3
Pin 14	P4	Data 4
Pin 15	P5	Data 5
Pin 16	P6	Data 6
Pin 17	P7	Data 7
Pin 18	P8	Data 8
Pin 19	P9	Data 9
Pin 20	P10	Data 10
Pin 21	P11	Data 11
Pin 22	P12	Data 12
Pin 23	P13	Data 13
Pin 24	P14	Data 14
Pin 25	P15	Data 15
Pin 26	GND	GND
Pin 27	P16	Data 16
Pin 28	P17	Data 17
Pin 29	P18	Data 18
Pin 30	P19	Data 19
Pin 31	P20	Data 20
Pin 32	ACT	Activity
Pin 33	P21	Data 21
Pin 34	P22	Data 22
Pin 35	P23	Data 23
Pin 36	P24	Data 24
Pin 37	P25	Data 25
Pin 38	P26	Data 26
Pin 39	P27	Data 27
Pin 40	P28	Data 28
Pin 41	P29	Data 29
Pin 42	P30	Data 30
Pin 43	P31	Data 31
Pin 44	GND	GND
Pin 45	P32	Data 32
Pin 46	P33	Data 33
Pin 47	P34	Data 34
Pin 48	P35	Data 35
Pin 49	VCC	+5V/1A
Pin 50	+12V	+12V/1A

J56 Extended LCD connector

Pin	Signal	Function
Pin 1	VCC	+5V
Pin 2	VGA-Red	
Pin 3	VGA-Green	
Pin 4	VGA-Blue	
Pin 5	VGA-Horiz.	Synch
Pin 6	VGA-Vert.	Synch
Pin 7	Shiftclock	
Pin 8	GND	Ground

J38 SCSI connector (50pin RM2.54), (if this option is assembled)

Pin	Signal	Pin	Signal
Pin 2	SCSI data 0	Pin 1	GND
Pin 4	SCSI data 1	Pin 3	GND
Pin 6	SCSI data 2	Pin 5	GND
Pin 8	SCSI data 3	Pin 7	GND
Pin 10	SCSI data 4	Pin 9	GND
Pin 12	SCSI data 5	Pin 11	GND
Pin 14	SCSI data 6	Pin 13	GND
Pin 16	SCSI data 7	Pin 15	GND
Pin 18	SCSI parity	Pin 17	GND
Pin 20	GND	Pin 19	GND
Pin 22	Terminator	Pin 21	GND
Pin 24	GND	Pin 23	GND
Pin 26	Terminator power	Pin 25	GND
Pin 28	GND	Pin 27	GND
Pin 30	GND	Pin 29	GND
Pin 32	SCSI ATN	Pin 31	GND
Pin 34	GND	Pin 33	GND
Pin 36	SCSI BUSY	Pin 35	GND
Pin 38	SCSI ACK	Pin 37	GND
Pin 40	SCSI Reset	Pin 39	GND
Pin 42	SCSI MSG	Pin 41	GND
Pin 44	SCSI Select	Pin 43	GND
Pin 46	SCSI CD	Pin 45	GND
Pin 48	SCSI REQ	Pin 47	GND
Pin 50	SCSI IO	Pin 49	GND

J40 Ethernet coax connector 10BASE-2, (only if this option is assembled)

Pin	Signal
Pin 1	EGND
Pin 2	Data

J31 Utility connector

Pin	Function
Pin 1	PS/2 Mouse Data
Pin 2	PS/2 Mouse Clock
Pin 3	PS/2 Keyboard Clock (front connector)
Pin 4	PS/2 Keyboard Data (front connector)
Pin 5	Keyboard Clock intern (needs Matrix Controller or jumper J46)
Pin 6	keyboard Data intern (needs Matrix Controller or jumper J45)
Pin 7	VCC
Pin 8	GND
Pin 9	Speaker Output
Pin 10	Stereo Sound Output Left (1.3W at 8Ω LM1877, since V2.2)
Pin 11	Stereo Sound Output Right (1.3W at 8Ω LM1877, since V2.2)
Pin 12	Ground for Sound Output
Pin 13	Microphone Input
Pin 14	VBAT
Pin 15	GND
Pin 16	Reset in

J77 Video ZV Port

Pin	Function
Pin 1	Video Port 0
Pin 2	Video Port 1
Pin 3	Video Port 2
Pin 4	Video Port 3
Pin 5	Video Port 4
Pin 6	Video Port 5
Pin 7	Video Port 6
Pin 8	Video Port 7
Pin 9	Video Port 8
Pin 10	Video Port 9
Pin 11	Video Port 10
Pin 12	Video Port 11
Pin 13	Video Port 12
Pin 14	Video Port 13
Pin 15	Video Port 14
Pin 16	Video Port 15
Pin 17	Ground
Pin 18	Serial Link Data I2C
Pin 19	Serial Link Clock I2C
Pin 20	Videoconverter Select
Pin 21	Horiz. Ref.
Pin 22	Vert. Ref.
Pin 23	Video Clock
Pin 24	Video Ready
Pin 25	Video Pixel Clock
Pin 26	VCC

J62 Video Input

Pin	Function
Pin 1	Video Input Channel 3 PAL or NTSC *
Pin 2	Video Input Channel 2 PAL or NTSC
Pin 3	GND
Pin 4	Video Input Channel 1 PAL or NTSC *
Pin 5	GND
Pin 6	Video Input for Y/C Sources, not used for PAL/NTSC

Since manualversion V2.26 VideoIN is corrected, as Philips chip differs to ITT in relation with the SAAINIT.EXE tool.

J67 MIDI / GAME Port

Pin	Function
Pin 1	VCC
Pin 2	Game Port A1
Pin 3	Game Port AX
Pin 4	GND
Pin 5	GND
Pin 6	Game Port AY
Pin 7	Game Port A2
Pin 8	VCC
Pin 9	VCC
Pin 10	Game Port B1
Pin 11	Game Port BX
Pin 12	MIDI OUTPUT
Pin 13	Game Port BY
Pin 14	Game Port B2
Pin 15	MIDI INPUT
Pin 16	not connected

J71 Audio Line Input

Pin	Function
Pin 1	Left Line Input
Pin 2	Ground
Pin 3	Right Line Input

J90 SOUND AUX connector, new since V2.2

	Pin	Signal
	Pin 1	Left
	Pin 2	Right

J1 Cooler Power and Feedback

Pin	Function
Pin 1	Ground
Pin 2	VCC
Pin 3	Feedback 5V TTL Signal (each turn of the fan should generate an impulse)

J58 Temperature connector, ext. NTC resi stor

Pin	Function
Pin 1	NTC resistor, e.g. 100 kΩ
Pin 2	NTC resistor, e.g. 100 kΩ

J97 Dual USB connector, NOT SUPPORTED by BIOS

Pin	Function
Pin 1	VCC
Pin 2	USB Port 0+
Pin 3	USB Port 0-
Pin 4	USB Port 1+
Pin 5	USB Port 1-
Pin 6	Ground

J95 AUI Interface connector, new since V2.3

	Pin	Signal
	Pin 1	+12V
	Pin 2	GND
	Pin 3	Collision +
	Pin 4	Collision -
	Pin 5	Receiver +
	Pin 6	Receiver -
	Pin 7	Transmitter +
	Pin 8	Transmitter -

- This signals must be isolated with a Ethernet transformator (PE64103 from Pulse Engineering or similar) and amplified with an National 8392C circuit for the coaxial connector.
  Please ask DesignIn Center of DIGITAL-LOGIC to get a sample schematics for the 10BASE-2 application.

J98 LAN LED connector, new since V2.3

	Pin	Signal
	Pin 1	BSE (cathode)
	Pin 2	BSE (anode), 470Ω resistor to Vcc included

J99 IDE HDD LED connector, new since V2.3

	Pin	Signal
	Pin 1	ACTP- (cathode)
	Pin 2	ACTP- (anode), 470Ω resistor to Vcc included

J102 POWER LED connector, new since V2.3

	Pin	Signal
	Pin 1	Vcc (anode)
	Pin 2	470Ω resistor to GND included

J96 Internal speaker, new since V2.3

	Pin	Signal
	Pin 1	Vcc
	Pin 2	Audio

J34/35 PC/104 BUS Interface

Pin	A:	B:	C:	D:
0			Ground	Ground
1	IOCHCK	Ground	SBHE	MEMCS16
2	SD7	RESET	LA23	IOCS16
3	SD6	+5V	LA22	IRQ10
4	SD5	IRQ9	LA21	IRQ11
5	SD4	NC	LA20	IRQ12
6	SD3	DRQ2	LA19	IRQ15
7	SD2	(-12V)	LA18	IRQ14
8	SD1	0WS	LA17	DACK0
9	SD0	+12V	MEMR	DRQ0
10	IOCHRDY	Ground	MEMW	DACK5
11	AEN	SMEMW	SD8	DRQ5
12	SA19	SMEMR	SD9	DACK6
13	SA18	SIOW	SD10	DRQ6
14	SA17	SIOR	SD11	DACK7
15	SA16	DACK3	SD12	DRQ7
16	SA15	DRQ3	SD13	+5 Volt
17	SA14	DACK1	SD14	MASTER
18	SA13	DRQ1	SD15	Ground
19	SA12	REF	Ground	Ground
20	SA11	SYSCLK		
21	SA10	IRQ7		
22	SA9	IRQ6		
23	SA8	IRQ5		
24	SA7	IRQ4		
25	SA6	IRQ3		
26	SA5	DACK2		
27	SA4	TC		
28	SA3	ALE		
29	SA2	+5 Volt		
30	SA1	OSC		
31	SA0	Ground		
32	Ground	Ground		

J65 PC/104+ BUS interface

Pin	A	B	C	D
1	GND/5.0V KEY2	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY2

Notes:
1. The shaded area denotes power or ground signals.
2. The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected to GND for shielding..

5.1 Jumpers on this MICROSPACE product

Jumper locations on the board

The figure shows the location of all the jumper blocks on the PCC-P5 board. The numbers shown in this figure are silk screened on the board so that the pins can easily be located. This chapter refers to the individual pin for these jumpers. The default jumper settings are written in bold. Be careful when you change some jumpers. Some jumpers are soldering jumpers so you need a miniature soldering station.

The Jumpers on the front side of the PCC-P5, (RM2.54mm jumpers)

J3, J4, J86	CPU Speed select	J3 (BF0)	J4 (BF1)	J86 (BF2)
	1.5 x CLK	**open**	**open**	**open**
	2 x CLK	closed	open	open
	2.5 x CLK	closed	closed	open
	3.0 x CLK	open	closed	open

Please see also table below for different CPU's and the correct BFx settings.

J7, J8	Clock selection	J7 (CLKSEL1)	J8 (CLKSEL0)
	CLK = 50 MHz	closed	closed
	CLK = 60 MHz	open	closed
	CLK = 66 MHz	**closed**	**open**

J52, J53	Direct VGA-BIOS select	J52	J53
	BIOS 0	**open**	**open**
	BIOS 1	closed	open
	BIOS 2	open	closed
	BIOS 3	closed	closed

Jumper	Signals	1-2 = open	2-3 = closed
J26	BIOS address SA16	**1-2 = recover mode**	2-3 = normal mode
J27	RTC reset	**open = run**	closed = reset
J37	SCSI-2 termination	**open = disable**	closed = enabled
J51***	2.9V CPU Support	open = 2.9V	**closed = normal 3,3V**
J59	PCI-BUS-Clock select (factory used)	open = pull up = 25Mhz	**closed = to PGOOD = 33Mhz**
J75	Generic Digital Input (factory used)	**open = pull up**	closed = pulldown
J76	Generic Digital Input (factory used)	**open = pull up**	closed = pulldown
J81 to J85	Memory data interface (factory used)	**open = pull up**	closed = pulldown

Position: Configuration	J41 IOS0	J42 IOS1	J43 IOS2		Base-Addr.	IRQ	Bus	Interface
0	closed	closed	closed		340	5	8	AUI/COAX/WS
1	**open**	**closed**	**closed**		**340**	**10**	**16**	**AUI/COAX/WS**
2	closed	open	closed		320	11	16	AUI/COAX/--
3	open	open	closed		300	5	8	AUI/COAX
4	closed	closed	open		340	5	8	10BASE-T/WS
5	open	closed	open		340	10	16	10BASE-T/WS
6	closed	open	open		320	11	16	10BASE-T/--
7	open	open	open		downloadable **software configuration**			

***** MMX CPU: J51 off and (U3 assembled and R173=51kW for 2.9V)**

The jumpers on the top- and bottom- side of the PCC-P5, (solder jumpers)

Parallel Port Address (default LPT1)

PCF1 (RTS1) R54 **	PCF0 (TXD1) J16 **	Port address	IRQ
low	Low 1-2	Disabled	7
Low	high 2-3	PS2 3BCh	7
High	**Low 1-2**	**LPT1 378h**	**7**
High	high 2-3	LPT2 278h	7

Parallel Port Mode (default normal)

ECPEN (MTR2) J15 **	PADCF (GAME) J14 **	Printer function
Low 1-2	**Low 1-2**	**Std. Printer Port, output only**
Low 1-2	High 2-3	Enh.Printer Port, bidirectional
High 2-3	Low 1-2	ECP
High 2-3	High 2-3	ECP & EPP

Jumper	Signals	1-2 = open	2-3 = closed
J09	External SMI event	**open = enabled**	close = disabled
J12**	Micro floppy drive select	1-2 = DRV B:	**2-3 = DRV A:**
J13**	Micro floppy drive select	1-2 = DRV B:	**2-3 = DRV A:**
J45	Keyboard Data	open = keymatrix	**closed = normal**
J46	Keyboard Clk	open = keymatrix	**closed = normal**
J54	LCD Voltage select	1-2 = 5V LCD	**2-3 = 3.3V LCD**
J55	VDD Save voltage	1-2 = 12V	**2-3 = 5V**
J57	CTAG10 select (factory setting)	**1-2 = to VIO**	2-3 = to GND
J63	Source the RTC from 3.3V for batteryless systems only	**open battery assembled**	closed = low batteryless
J68**	Audio configuration (not used)	**open**	
J69**	Audio configuration (not used)	**open**	
J78	VGA Power AVCC,IVCC, SVCC	1-2 = 5V	**2-3 = 3.3V**
J79	VGA Powersupply Bus BVCC	1-2 = 5V	**2-3 = 3.3V**
J80	VGA Powersupply Memory MVCC	1-2 = 5V Memory	**2-3 = 3.3V Memory**
J87	Memory supply, new since V2.2	1-2 = +5V	**2-3 = 3.3V**
J89	GPO0 mode, not supported	**open**	closed
J92	COM1 select	**RS232**	RS422/485
J94	COM2 select	**RS232**	RS422/485
J100	Audio configuration mode	external	**standard**
J101	Audio configuration mode EEPROM	internal	**external**

**** only on old version PCC-P5 V2.1a**

Settings written in bold are defaults!

5.1.1 CPU core voltages selection, (since V2.2)

For INTEL P5-166Mhz select 3.3V
For INTEL P5-200Mhz select 2.9V
For AMD K6-2-266Mhz select 2.0V

J88:

V-ID4 Pos: 9-10	V-ID3 Pos: 7-8	V-ID2 Pos: 5-6	V-ID1 Pos: 3-4	V-ID0 Pos: 1-2	Rated Output CPU Core Voltage
Close	open	open	open	open	1.30 V
Close	open	open	open	Close	1.35 V
Close	open	open	Close	open	1.40 V
Close	open	open	Close	Close	1.45 V
Close	open	Close	open	open	1.50 V
Close	open	Close	open	Close	1.55 V
Close	open	Close	Close	open	1.60 V
Close	open	Close	Close	Close	1.65 V
Close	Close	open	open	open	1.70 V
Close	Close	Open	open	Close	1.75 V
Close	Close	Open	Close	open	1.80 V
Close	Close	Open	Close	Close	1.85 V
Close	Close	Close	open	open	1.90 V
Close	Close	Close	open	Close	1.95 V
Close	Close	Close	Close	open	2.00 V
Close	Close	Close	Close	Close	2.05 V
Open	open	open	open	open	Shutdown 0.0V
Open	open	open	open	Close	2.10 V
Open	open	open	Close	open	2.20 V
Open	open	open	Close	Close	2.30 V
Open	open	Close	open	open	2.40 V
Open	open	Close	open	Close	2.50 V
Open	open	Close	Close	open	2.60 V
Open	open	Close	Close	Close	2.70 V
Open	Close	open	open	open	2.80 V
Open	Close	Open	open	Close	2.90 V
Open	Close	Open	Close	open	3.00 V
Open	Close	Open	Close	Close	3.10 V
Open	Close	Close	open	open	3.20 V
Open	Close	Close	open	Close	3.30 V
Open	Close	Close	Close	open	3.40 V
Open	Close	Close	Close	Close	3.50 V

BFx-Settings for different CPU's.

BF0	BF1	BF2	BUS	CLK	INTEL P1	MMX	MMX-L	AMD-K6	AMD-K6
1	0	1		200	3.0	3.0		3.0	3.0
0	0	1		166	2.5	2.5	4.0	2.5	2.5
0	1**	1		133	2.0	2.0**		2.0	2.0 or 6.0*
1	1**	1		100/233	1.5	1.5**/3.5		3.5	3.5
1	0	0		333				5.0	5.0
0	0	0					2.5	4.5	4.5
0	1	0		266/300				4.0/4.5	4.0/4.5
1	1	0		366				5.5	5.5

* Model 8 (F:8)
** MMX (330Ω pull up {MSM-P5})
1 OPEN jumper
0 CLOSED jumper

Remarks: AMD's need a customized BIOS.

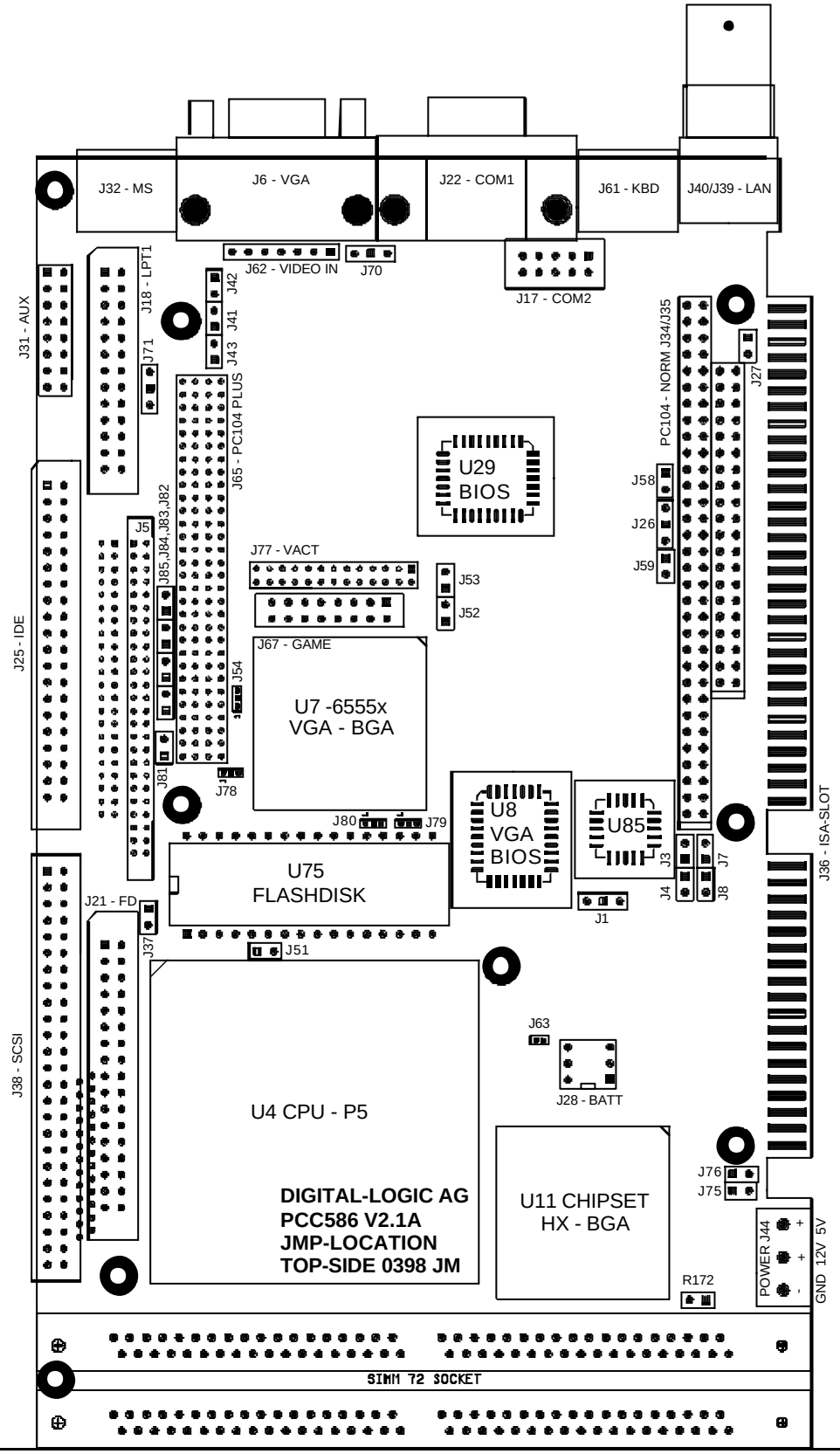
NEW VGA BIOS SELECTION: (needs a 16multibios):

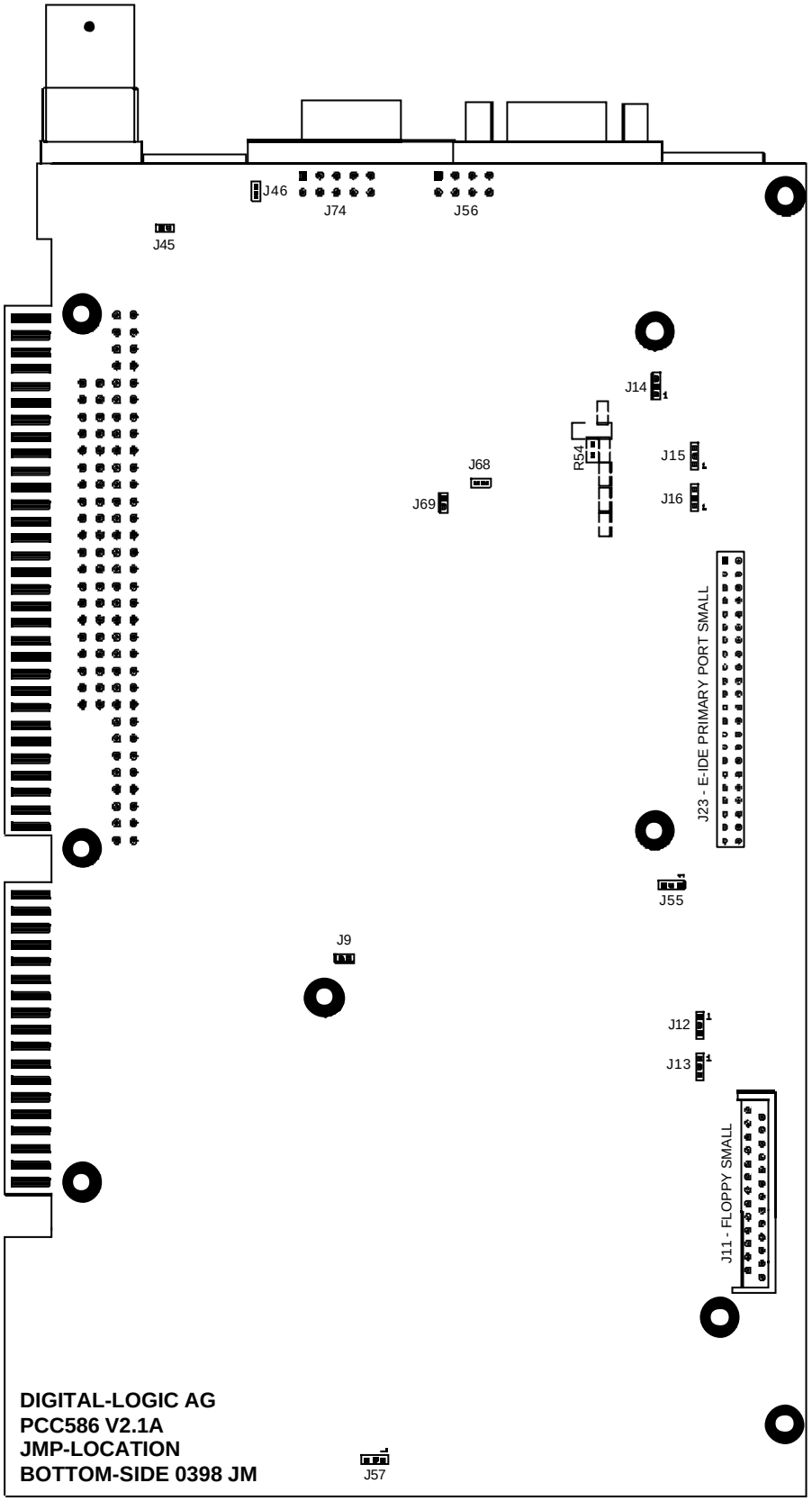
J82-J85	Direct VGA-BIOS select	J85	J84	J83	J82
CRT	BIOS 0	**open**	**open**	**open**	**open**
LCD 1	BIOS 1	open	open	open	close
LCD 2	BIOS 2	open	open	close	open
LCD 3	BIOS 3	open	open	close	close
LCD 4	BIOS 4	open	close	open	open
LCD 5	BIOS 5	open	close	open	close
LCD 6	BIOS 6	open	close	close	open
LCD 7	BIOS 7	open	close	close	close
LCD 8	BIOS 8	close	open	open	open
LCD 9	BIOS 9	close	open	open	close
LCD 10	BIOS 10	close	open	close	open
LCD 11	BIOS 11	close	open	close	close
LCD 12	BIOS 12	close	close	open	open
LCD 13	BIOS 13	close	close	open	close
LCD 14	BIOS 14	close	close	close	open
LCD 15	BIOS 15	close	close	close	close

Settings written in bold are defaults!

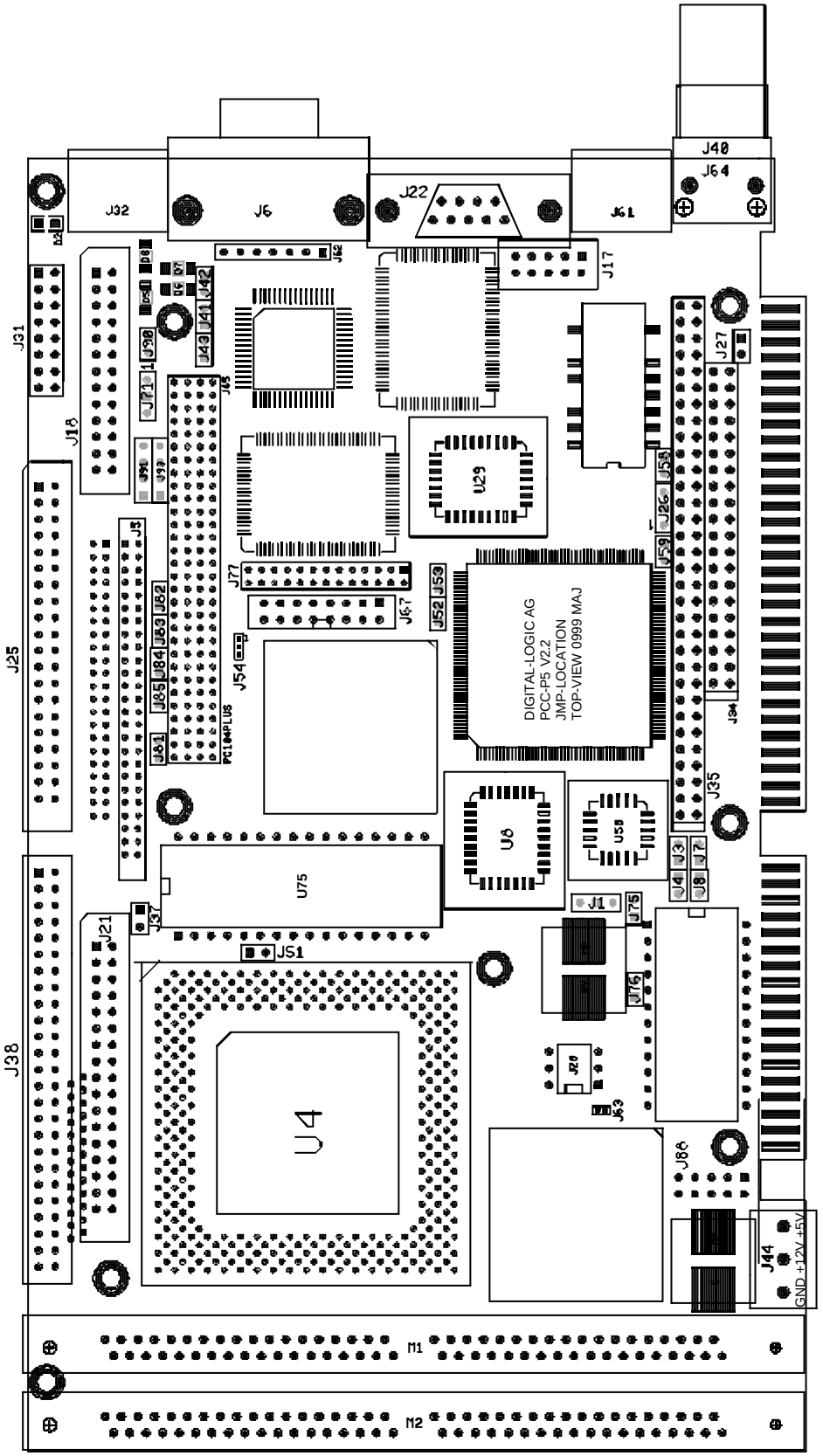
5.2 Jumper and Connector Locations

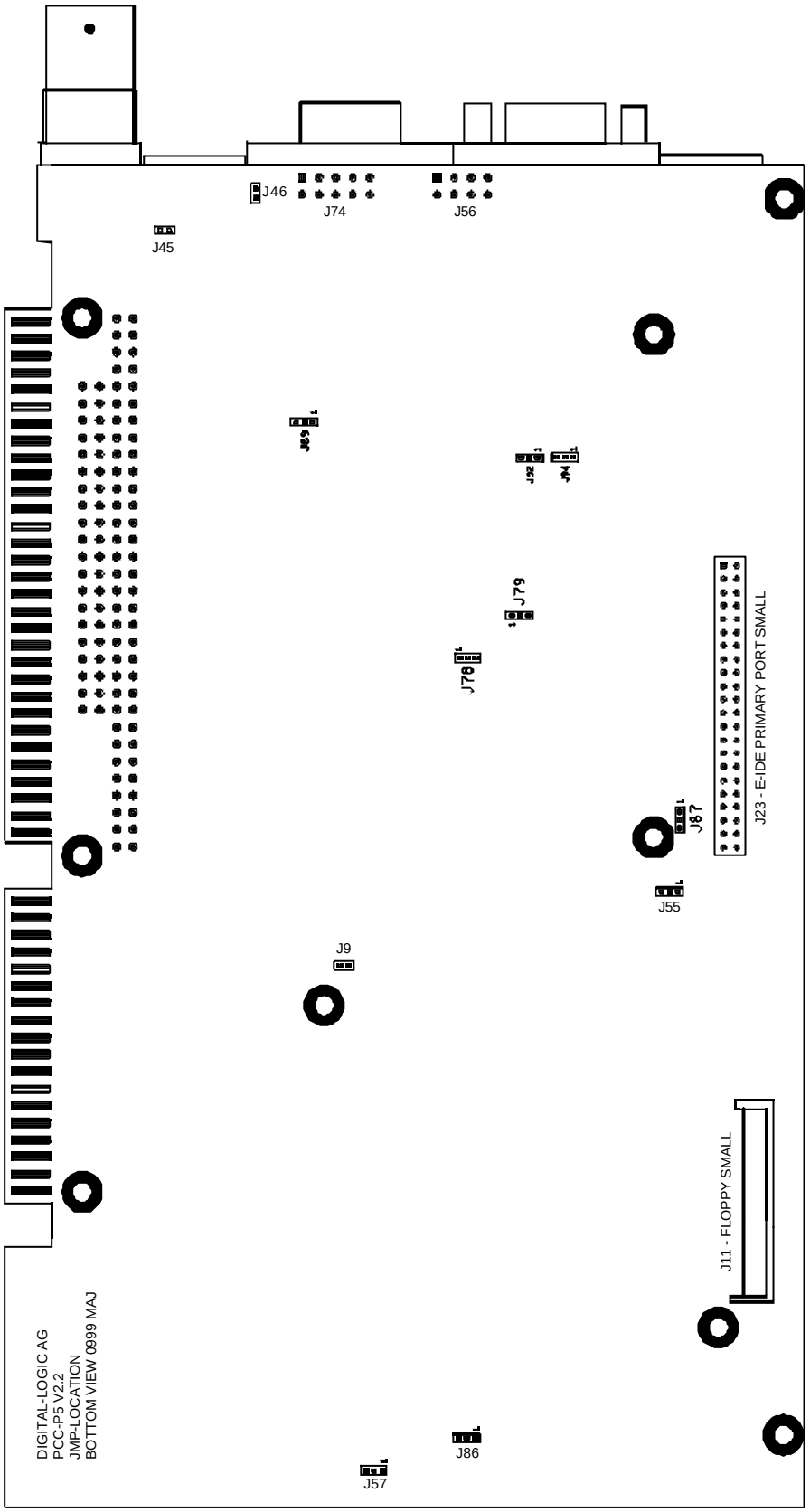
5.2.1 PCC-P5 V2.1




J46
J74
J56
J45
J14
J68
J69
R54
J15
J16
J23 - E-IDE PRIMARY PORT SMALL
J55
J9
J12
J13
J11 - FLOPPY SMALL
DIGITAL-LOGIC AG
PCC586 V2.1A
JMP-LOCATION
BOTTOM-SIDE 0398 JM
J57

5.2.2 PCC-P5 V2.2




J46
J74
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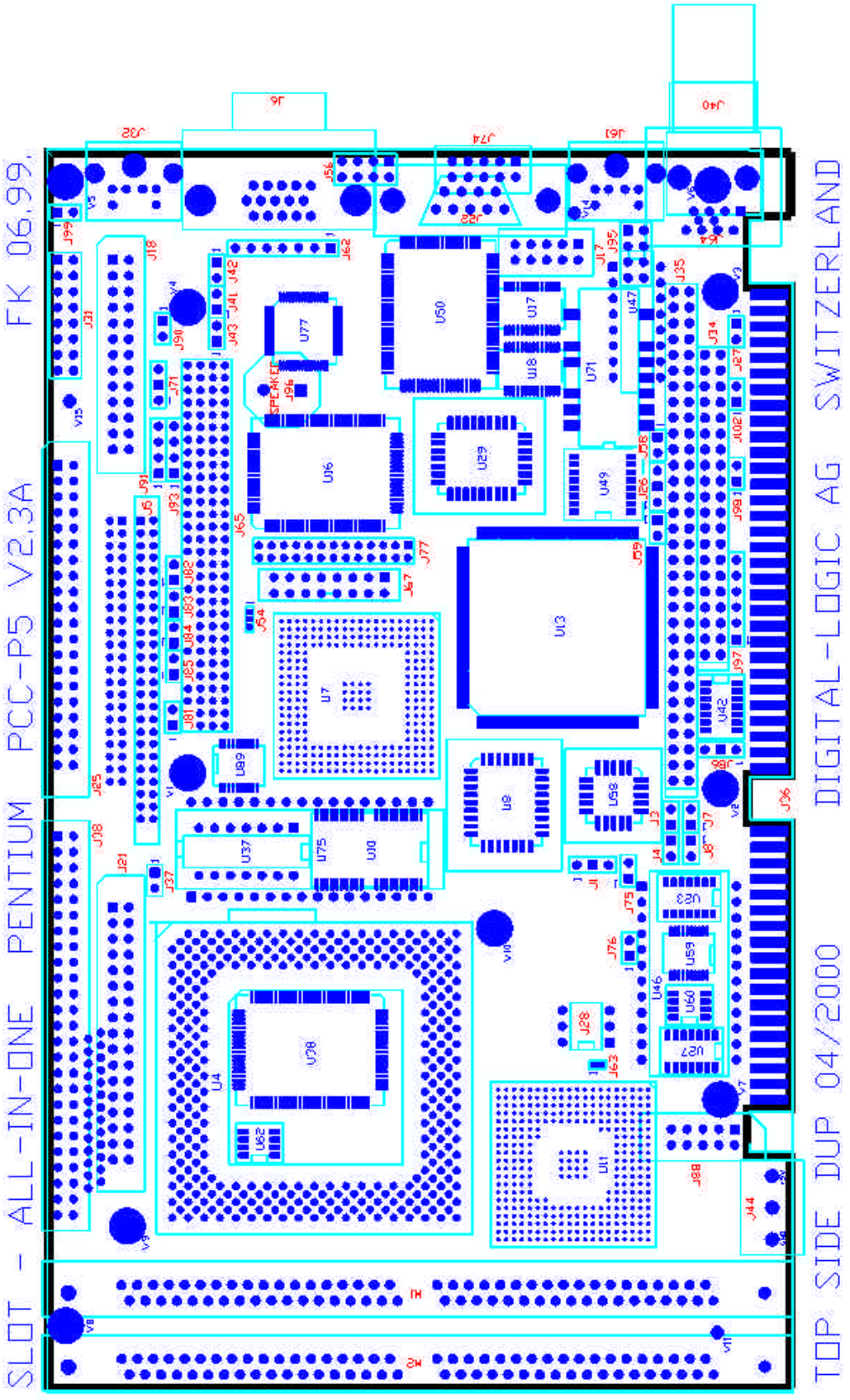
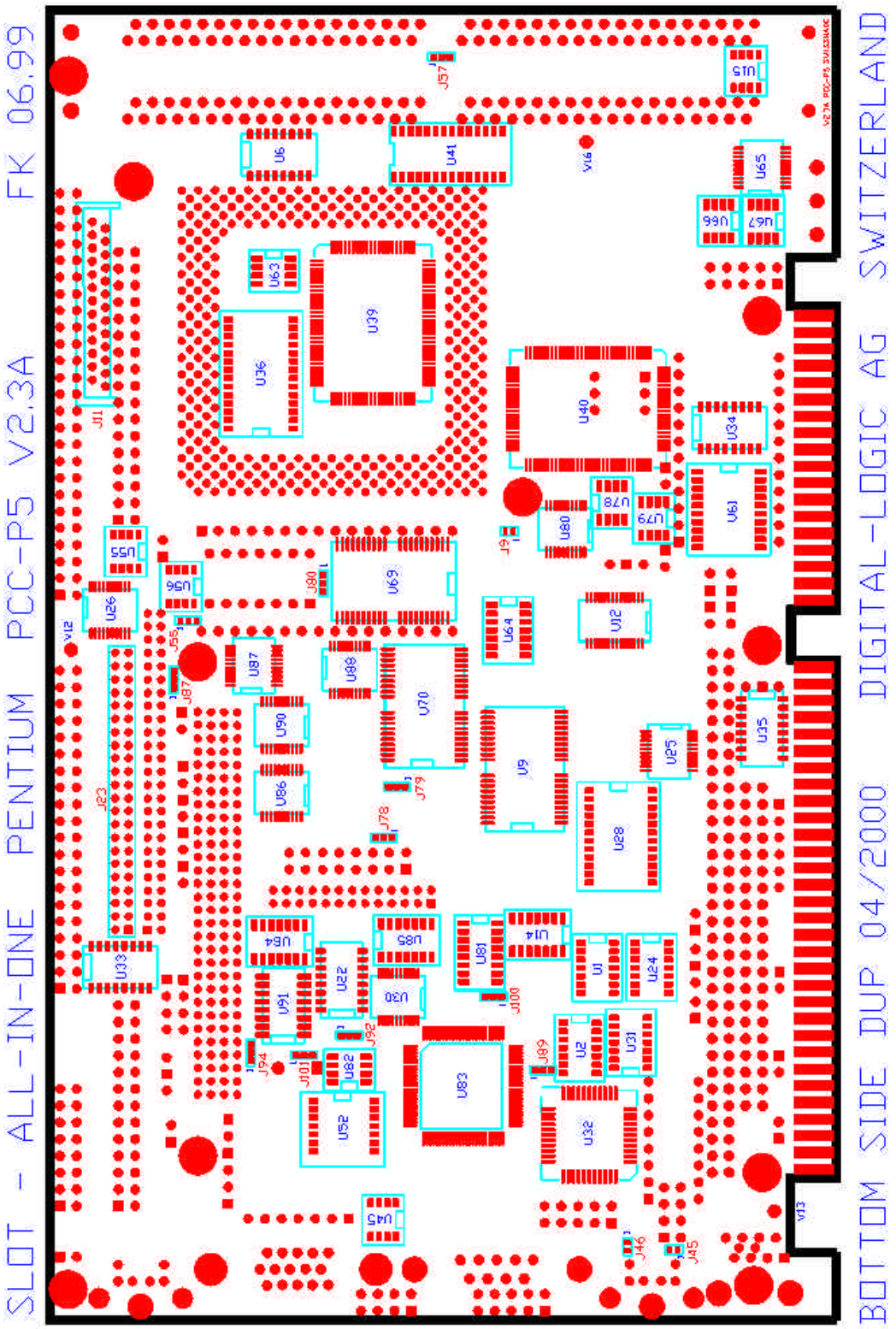
J45
J69
J32
J4
J79
J78
J87
J23 - E-IDE PRIMARY PORT SMALL
J55
J9
J11 - FLOPPY SMALL
J86
J57
DIGITAL-LOGIC AG
PCC-P5 V2.2
JMP-LOCATION
BOTTOM VIEW 0999 MAJ

5.2.3 PCC-P5 V2.3




SLOT - ALL-IN-ONE PENTIUM PCC-P5 V2.3A FK 06.99
BOTTOM SIDE DUP 04/2000 DIGITAL-LOGIC AG SWITZERLAND

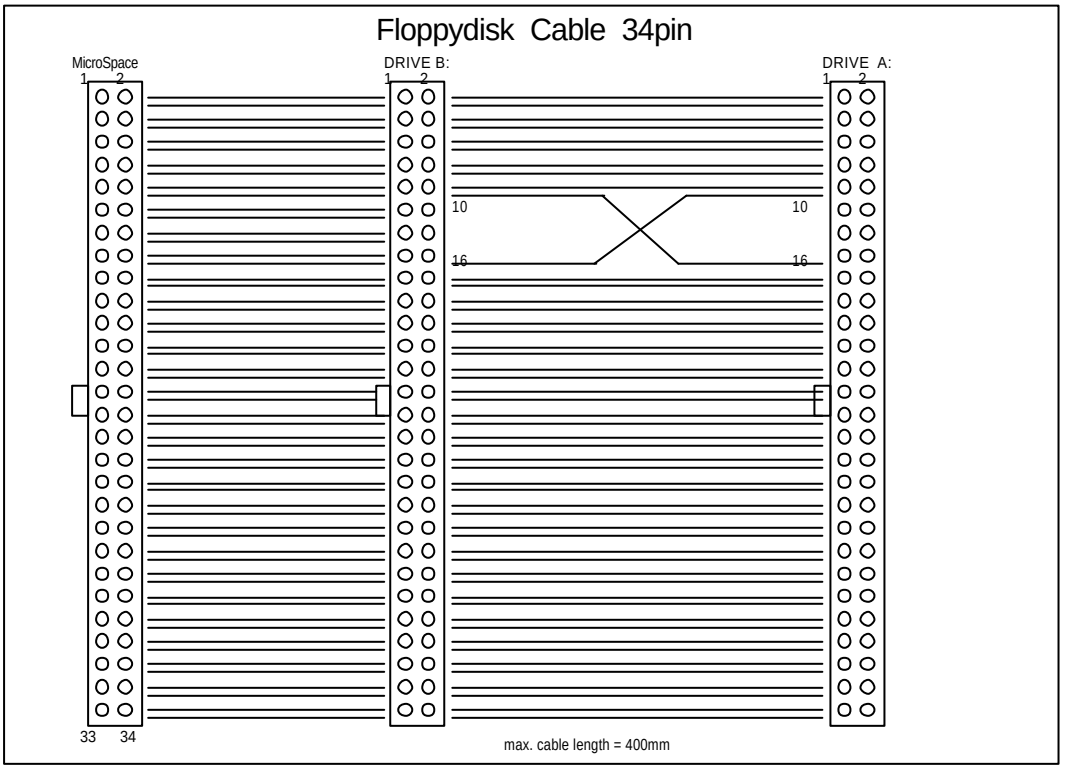
6 LED CRITERIONS:

LED	Color	Function
D2	Red	Primary HDD
D5	Red	LAN TX
D6	Red	LAN RX
D7	Red	LAN linked
D8	Red	LAN busy
D9		Not defined

7 CABLE INTERFACE

7.1 The Floppy Disk Cable

IDT Terminal for Dual Row 0.1" (2.54 mm grid) and 1.27 mm flat cable



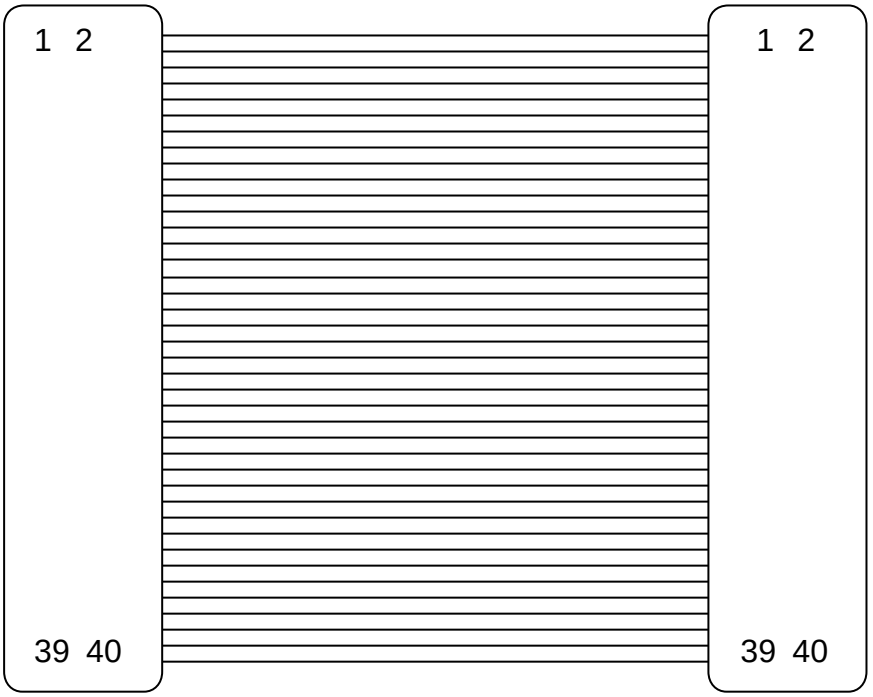
For drive A: the lines 10 to 16 are crossed (180 degrees).

All floppy drives must be selected as drive number 2, because the cable assigns the drive letter A: or B: to the drives. The power must be connected separately. Refer to the technical manual of the floppy drives used.

The last drive must be terminated with 1 kohms. Do not use 150 ohms terminated floppy drives!

7.2 The Harddisk Cable 40 pins

IDT terminal for dual row 0.1" (2.54 mm grid) and 1.27 mm flat cable. 40 pins signal, power is separately wired. Refer to the technical manual of the harddisk used.



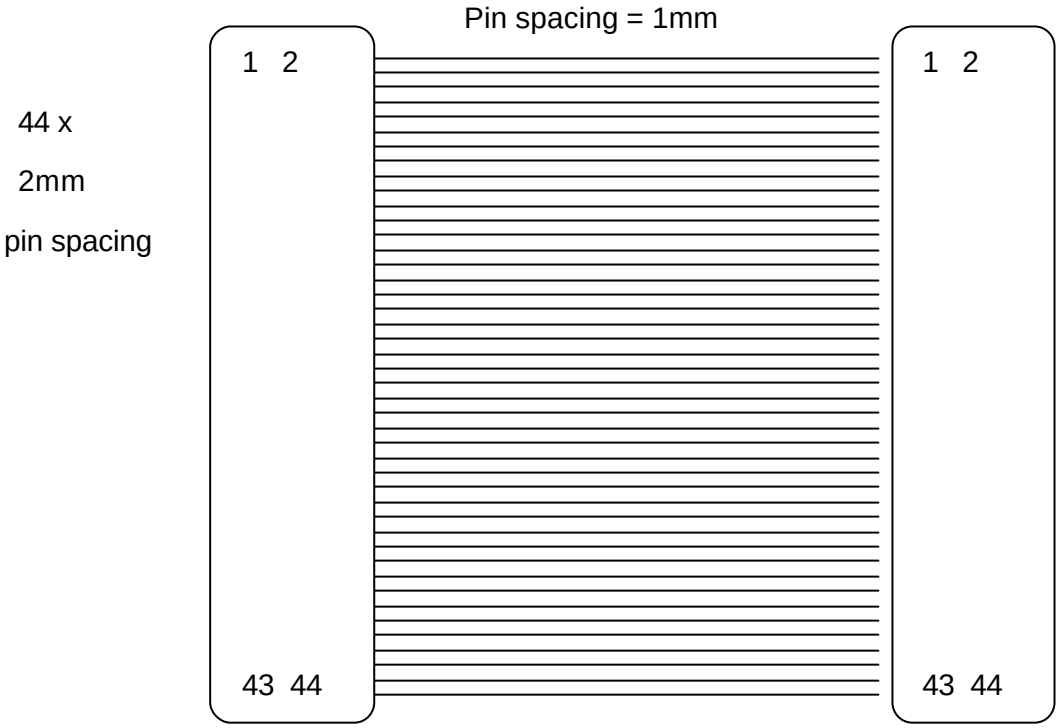
Max. length for IDE cable is 30 cm.

ATTENTION:

A maximum of two IDE drives can be connected to the HD-Interfaces. The first drive must always be the MASTER drive (= C:) and the second is the SLAVE drive. Check the selection of the drive in the technical manual. An inverse connection could destroy the drive or the MICROSPACE PCC-P5. Be very careful. There is no warranty in this case.

7.3 The Harddisk Cable 44 pins

IDT Terminal for Dual Row (2.00 mm grid) and 1.00 mm flat cable. 44 pins = 40 pins signal and 4 pins power.

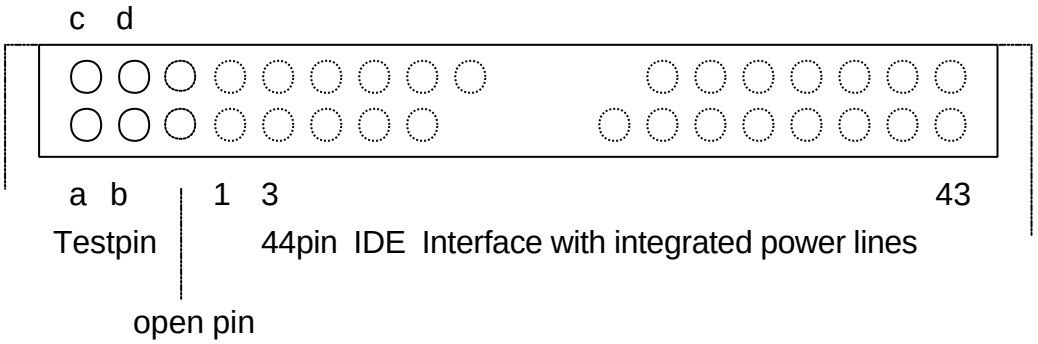


Max. length for the IDE cable is 30 cm.

ATTENTION:

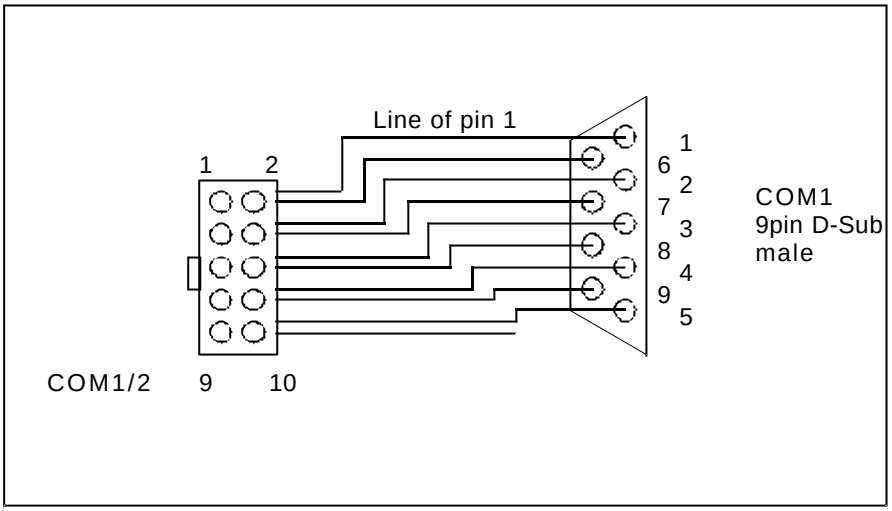
Check the pin 1 marker of the cable and the connector before you power-on. See the technical manual of the drives used, because a wrong cable will immediately destroy the drive and/or the MICROSPACE PCC-P5 board. There is no warranty in this case. Without the technical manual you cannot connect this type of drive.

The 44 pins IDE connector on the drives are normally composed of the 44 pins and 2 open pins and 4 test pins, total: 50 pins. Leave the 4 test pins unconnected .



7.4 The COM 1/2 Serial Interface Cable

DT terminal for dual row 0.1" (2.54 mm grid) and 1.27 mm flat cable



ATTENTION:

- Do not short-circuit these signal lines.
- Never connect any pins either to the same plug or to any other plug on the MICROSPACE PCC-P5. The +/-10Volt will destroy the MICROSPACE core logic immediately. No warranty in this case!
- Do not overload the output: max. output current of Maxim converters: 10 mA
- The maximum supply current for the mouse is ~ 5mA!

8 SPECIAL PERIPHERALS, OPTIONAL FUNCTIONS

8.1 Special Peripherals

8.1.1 Multifunction latch

The multifunction latch allows control over several functions such as powerdown, contrast and watchdog. This latch can be controlled by the application program.

Latch 1: Programing address is: 2B0 hex (write only)

PCC-P5	Function:	Bit Number:
Watch DOG Enable	Enable	0
Serial EEPROM Data	Data Out (to the EEPROM)	1
NC	NC	2
Temperatur Controller	Data Out (to the Controller)	3
Temperatur Controller	Shift clock	4
EEPROM	Shift clock	5
EEPROM	Chipselect CS	6
LED	0=On, 1=Off	7

Latch 2: Programing address is: 2B0 hex (read only)

PCC-P5	Function:	Bit Number:
Serial EEPROM Data	Data In (from the EEPROM)	0
Heatclock	Temp. Measurement	1
Temperatur Controller	Data In (from the Controller)	2
Temperatur Controller	OutputSignal	3
NC		4
NC		5
NC		6
NC		7

9 ETHERNET LAN

9.1 Ethernet IO-Address and IRQ selection

The Ethernet interface is configured with the values stored in an EEPROM. The default values are:

Jumper Configuration	J41 IOS0	J42 IOS1	J43 IOS2		Base address	IRQ	BUS	INTERFACE
0	closed	closed	closed		340	5	8	AUI/COAX
1	**open**	**closed**	**closed**		**340**	**10**	**16**	**AUI/COAX**
2	closed	open	closed		320	11	16	AUI/COAX
3	open	open	closed		300	2/9	8	AUI/COAX
4	closed	closed	open		340	5	8	10BASE-T
5	open	closed	open		340	10	16	10BASE-T
6	closed	open	open		320	11	16	10BASE-T
7	open	open	open		Software downloadable configuration			

On the board, the default configuration and the selected configuration are labeled. The label also contains the unique node address:

Label example:

```
NODE:   aabbccddeeff            TYPE: B
  0     340     i5      8       AUI
  1     340     i10     16      AUI
* 2     320     i11     16      AUI
  3     300     i5      8       AUI
  4     340     i5      8       10BASE-T
  5     340     i10     16      10BASE-T
  6     320     i11     16      10BASE-T
```

The asterisk * in front of the configuration 2 line marks the selected configuration. You can change the hardware configuration by modifying the jumper IOS0 - IOS2.

The software downloaded configuration ise recommended only for custom cases, where the values must be altered, without soldering the jumpers onboard. The downloaded configuration works only with Novell V3.11 and Novell Lite and all other ODI driver NOS.

For OS/2, NT and UNIX applications always use the hardware configuration, because the drivers are adapted only for hardware configuration schemes.

9.2 Ethernet hardware configuration

The Ethernet controller is hardware selectable with preprogrammed values from the EEPROM. This is the normal way to start with all operating systems and NOS.

A. Select the configuration

Selected using the IOS0 - IOS2 jumper.
Refer to the table in the previous chapter.

! RESTART THE PC SYSTEM TO INITIALIZE THE NEW CONFIGURATION !

B. Generate the corresponding NET.CFG file

The NET.CFG file can be altered or created using a normal ASCII editor or with the tools from Digital-Logic. This step must be taken at the beginning or after **selecting a new configuration.**

BCONF	Create the correct NET.CFG files

C. Starting the Network driver on the workstation: for NW3.11

The following drivers and files are available on the tool disk.
Start the following files in this order (include in the Autoexec.bat file)

LSL	low level driver
SMC90000	SMC Driver for Novell V3.11
IPXODI	IPX- ODI Driver
NETX	Novell Network Shell

Now you can login with your password.

D. Starting the Network driver on the workstation: for Novell Lite

On the tool disk the following drivers and files are available.
Start the following files in this order (include in the Autoexec.bat file)

LSL	low level driver
SMC90000	SMC Driver for Novell V3.11
IPXODI	IPX-ODI Driver
CLIENT	Lite V1.1 Workstation Shell

Now you can login with your password.

9.3 Utilities for programming EEPROM and DIAGNOSTICS

The EEPROM is factory programmed with the default values shown in chapter 3. If the node address should be modified, use a program utility.

Use this program to store the standard defaults in the EEPROM:

ETHPROG.EXE — Store the default value for IOBase, IRQ in the EEPROM and ask for the node address number and store it also.

If the ETHPROG hangs on the address 400hex, the SMC91C92 is not accessable. Take the following steps:

1. Select the CONFIGURATION 7 (IO x Jumpers)
2. Restart the system
3. Start ETHPROG.EXE and enter the node address
4. Select the desired CONFIGURATION x (IO x Jumpers)
5. Restart the system
6. Use BCONF to produce the new NET.CFG file

Use these programs for custom modification in the EEPROM:

PRO9000.EXE — Enables you to modify every value in the EEPROM. Check the SMC91C94 datasheet for the register functions.

NETCONF.EXE — Programs also the EEPROM with defaults or custom values.

To program the EEPROM defaults and node address, follow the steps:

1. Select the CONFIGURATION 7 (IO x Jumpers)
2. Restart the system
3. Start NETCONF.EXE and use the menu store defaults
4. Select the desired CONFIGURATION x (IO x Jumpers)
5. Restart the system
6. Use BCONF to produce the new NET.CFG file

Use this program for diagnostics:

SCECR.EXE — 91C94 diagnostic tools

9.4 Ethernet-Drivers

➔ **Download the latest drivers at** http://www.smsc.com **or** http://www.digitallogic.com

9.4.1 INT 15h SFR Functions

All functions are performed by starting the SW-interrupt 15hex with the following arguments:

Function:	**WRITE TO EEPROM**	
Number:	E0h	
Description:	Writes the Data byte into the addressed User-Memory-Cell from the serial EEPROM. The old value is automatically deleted.	
Input Values:	AH = E0h	Function Request AL Databyte to store BX Address in the EEPROM (0-1024 Possible) SI 1234h User-Password (otherwise EEP is write-protected) DLAG-Password for access to the DLAG-Memory-Cells
Output Values:	None, all registers are preserved.	

Function:	**READ FROM EEPROM**	
Number:	E1h	
Description:	Reads the Data byte from the addressed User-Memory-Cell of the serial EEPROM.	
Input Values:	AH = E1h	Function Request BX Address in the EEPROM (0-1024 Possible) SI 1234h User-Password DLAG-Password for access to the DLAG-Memory-Cells
Output Values:	AL	read databyte

Function:	**WRITE SERIALNUMBER**	
Number:	E2h	
Description:	Writes the Serialnumber from the serial EEPROM into the addressed DLAG-Memory-Cell. The old value is automatically deleted.	
Input Values:	AH = E2h	Function Request DX,CX,BX Serialnumber (Binary, not Ascii) SI Password
Output Values:	None, all registers are preserved.	

Function:	**READ SERIALNUMBER**	
Number:	E3h	
Description:	Reads the serialnumber from the board into the serial EEPROM.	
Input Values:	AH = E3h	Function Request

Output Values:	DX,CX,BX	Serialnumber (Binary, not Ascii)

Function:	**WRITE PRODUCTION DATE & RESET DLAG-COUNTERS**	
Number:	E4h	
Description:	Writes the production date into the addressed DLAG-Memory-Cell from the serial EEPROM. The old value is automatically deleted. If the Password is also in DX, the counters will be resettet (=0).	
Input Values:	AH = E4h	Function Request
	BX	Year (1997 => BH=19, BL=97)
	CH	Month (1..12)
	CL	Day of Month (1..31)
	SI	Password
	DX	Password, if counters should be resetted, otherwise no password.
Output Values:	None, all registers are preserved.	

Function:	**READ PRODUCTION DATE**	
Number:	E5h	
Description:	Reads the production date from the board in the serial EEPROM.	
Input Values:	AH = E5h	Function Request
Output Values:	BX	Year (1997 => BH=19, BL=97)
	CH	Month (1..12)
	CL	Day of Month (1..31)

Function:	**CHANGE VALUE IN KEYMATRIX**	
Number:	E6h	**NOT AVAILABLE ON THIS BOARD!**
Description:	Writes the data byte into the Keymatrix table from the EEPROM.	
Input Values:	AH = E6h	Function Request
	AL	New Value to store in the table
	BX	Address in the Keymatrix table in the EEPROM
Output Values:	None, all registers are preserved.	

Function:	**TRANSFER KEYMATRIX TO EEPROM**
Number:	E7h **NOT AVAILABLE ON THIS BOARD!**
Description:	Transfers the Keymatrix table from the Keyboard controller to the serial EEPROM.
Input Values:	AH = E7h Function Request
Output Values:	None, all registers are preserved.

Function:	**WRITE INFO2 TO THE EEPROM**
Number:	F0h (PHOENIX) E8h (AMI)
Description:	Writes the information bytes into the serial EEPROM.
Input Values:	AH = F0h Function Request (PHOENIX) AH = E8h Function Request (AMI) AL Board Type (M= PC/104, E=Euro, W=MSWS, S=Slot, C=Custom) DI CPU Type (1=ELAN310, 2=ELAN400, 3=486SLC, 4=486DX, 5=P5) BX Board Version (Ex: V1.5 => BH=1, BL=5) CX BIOS Version (Ex: V3.0 => CH=3, CL=0) DH Number of 512k Flash DL Number of 512k SRAM SI Password
Output Values:	None, all registers are preserved.

Function:	**READ INFO2 FROM THE EEPROM**
Number:	E9h
Description:	Reads the information bytes out of the serial EEPROM.
Input Values:	AH = E9h Function Request
Output Values:	AL Board Type (M= PC/104, E=Euro, W=MSWS, S=Slot, C=Custom) DI CPU Type (1=ELAN310, 2=ELAN400, 3=486SLC, 4=486DX, 5=P5) BX Board Version (Ex: V1.5 => BH=1, BL=5) CX BIOS Version (Ex: V3.0 => CH=3, CL=0) DH Number of 512k Flash DL Number of 512k SRAM

Function:	**READ INFO3 FROM THE EEPROM**
Number:	EAh
Description:	Reads the information bytes out of the serial EEPROM.
Input Values:	AH = EAh Function Request
Output Values:	AX counter of BOOTERRORS counter of SETUP ENTRIES counter of LOW BATTERY ERROR counter of BOOT UP SYSTEM

Function:	**WATCHDOG**
Number:	EBh
Description:	Enables, strobes and disables the WATCHDOG. After power-up, the Watchdog is always disabled. Once the Watchdog has been enabled, the user application must perform a strobe at least every 800ms, other- wise the watchdog performs a hardware reset.
Input Values:	AH = EBh Function Request AL 00 Disable Watchdog 01..FE Enable Watchdog FF Strobe Watchdog
Output Values:	None, all registers are preserved.

Function:	**READ TEMPERATURE OF LM75**
Number:	ECh **NOT AVAILABLE ON THIS BOARD!**
Description:	Reads the temperature from the LM75.
Input Values:	AH = ECh Function Request
Output Values:	AL temperature BL 00 =>value OK, otherwise NOK

Function:	**SET POWERSAVE**
Number:	EDh
Description:	Sets Powersave options.
Input Values:	AH = EDh Function Request AL 00 => LCD Powersave BL Bit 2 LCD-VDD on/off NOT AVAILABLE Bit 1 LCD-VEE on/off NOT AVAILABLE Bit 0 LCD-Backl. on/off NOT AVAILABLE 01 => HD0 Powersave AVAILABLE BL 0 The drive will immediately go to the Standby mode. 1 The drive will immediately go to the active mode. 2 The drive will immediately go to the standby mode. If the sector count registers is zero then the timer will be disabled. If the sector count register is non-zero the timer will be enabled and initialized with the sector count value. 3 The drive will immediately go to the active mode.If the sector count registers is zero then the timer will be disabled. If the sector count register is non-zero the timer will be enabled and initialized with the sector count value. 5 If the drive is in active mode, the sector count registers will be set to 0FFh. If the drive is in, going to, or recovering from the standby mode, the sector count register will be set to 000h. 6 The drive enters the sleep mode. Either a soft- or hardware reset is required to recover from this mode. The drive will then go to the standby mode. 02 => HD1 Powersave BL Same as HD0 Powersave
Output Values:	None, all registers are preserved

Function:	**LED SWITCH-STATUS**	
Number:	EEh	**NOT AVAILABLE ON THIS BOARD!**
Description:	Sets LED and reads the switches.	
Input Values:	AH = EEh	Function Request AL 01 Set LEDs only 02 Reads Switches only 03 Set LEDs and read Switches BL Only for Set LED mode used LEDs Bit X is LED X
Output Values:	AL	Switches, if mode is set, otherwise all registers are preserved.

Function:	**INFORMATION ABOUT INT15-SUPPORT ON THE BOARD**	
Number:	EEh	
Description:	Gives informations about the supported interrupt 15 functions.	
Input Values:	AH = EFh	Function Request AL Number of Interrupt, where you need information SI Password, if you want information about a password saved Interrupt
Output Values:	BX	Interrupt-Information Word BH Version number of Interrupt (0 = not supported) If there is a Password-saved Interrupt, a zero is shown, if the password is wrong. BL Second-Version number.

10 SCSI INTERFACE (OPTION)

Please note, that the option SCSI-2 is not available on the SCSI connector J38, as these additional data signals are not connected to this connector.

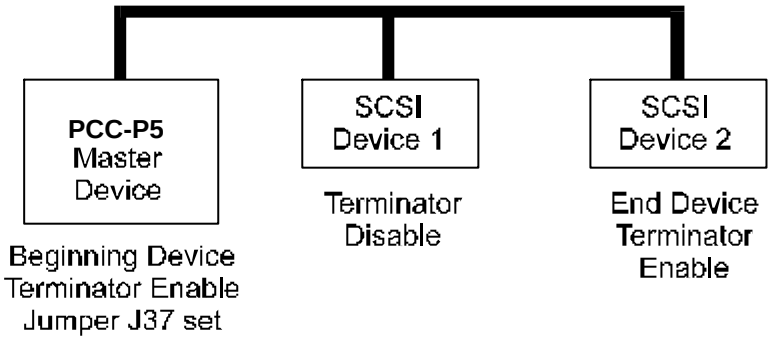
The SCSI-2 interface is realized with the NCR 53C810 controller. This chip is fully supported by NCR SCSI Device Management System (SDMS) software, that supports the Advanced SCSI Protocol Interface (ASPI) and the ANSI Common Access Method (CAM). The NCR 53C810 operates the SCSI bus at 5 MB/s asynchronously or 10 MB/s synchronously, and bursts data to the host at full PCI speed up to 110 MB/s (at 33 MHz).

The SCSI-2 controller has full PnP recognition, a 64-Byte DMA FIFO and all SCSI signals are ESD protected up to 2 kV.

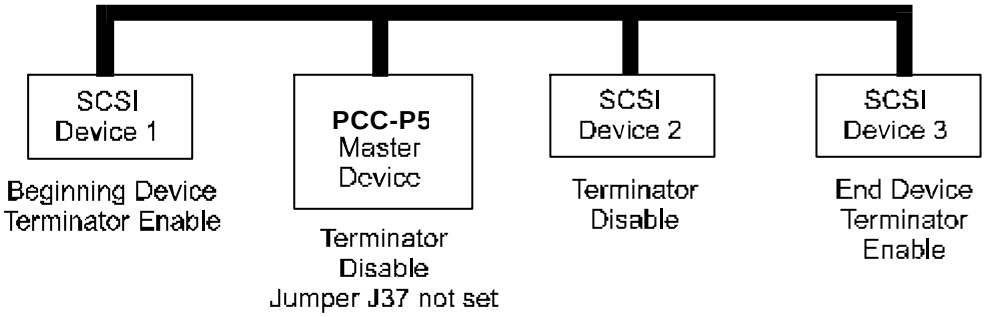
The user can connect up to 7 SCSI devices to the NCR 53C810, all the SCSI devices are daisy chained trough one SCSI-Bus cable. This cable must have terminators at both ends; i.e. the beginning device and end device. Without proper installation of the terminators it will cause a SCSI devices malfunction. On the PCC-P5 board the terminator is active, when jumper J37 is set.

The following figures illustrate where the terminators can be placed:

Example 1:



Example 2:



The boot devices on the SCSI-2 interface:

- any SCSI-2 harddisk
- CD drives
- Syquest removable media
- Tapes, MO- and ZIP-Drives

- Until boardversion V2.1, the SCSI extension had to be programmed into the U75 (EPROM)
- Since boardversion V2.2, SCSI extension is programmed within the core BIOS.

10.1 SCSI Drivers for operating system support

Current SYMBIOS LOGIC PCI SDMS Drivers:

Environment	Drivers	Version	Date
DOS 3.0	DOSCAM.SYS	DOSCAM-3.05.00	05/08/95
	SCSIDISK.SYS	SCSIDISK-3.03.00	09/28/94
	CDROM.SYS	CDROM-3.03.00	09/08/94
	ASPICAM.SYS	ASPICAM-3.03.00	10/31/94
	MINICAM.SYS	MINICAM-3.02.00	10/31/94
	INSTALL.EXE	PROSCSI-3.01.00	10/31/94
DOS 4.0	ASPI8XX.SYS	ASPI8XX-4.01.00	11/20/95
	SYMDISK.SYS	SYMDISK-4.01.00	11/13/95
	SYMCD.SYS	SYMCD-4.01.00	10/03/95
	INSTALL.EXE	8xxINSTALL-4.01.00	12/15/95
OS/2	OS2CAM.ADD	OS2CAM-3.03.00	02/05/95
Windows NT 3.1	NCRSDMS.SYS	NCRSDMS.SYS	12/06/94
Windows NT 3.5	SYMC8XX.SYS	DULUTH-2.00.00	08/25/95
Windows 95	SYMC8XX.MPD	DULUTH-2.00.00	08/25/95
SCO Unix	BTLD	BTLDPCI-3.05.00	10/25/95
Netware v. 3.1x	SDMSNET3.DSK	SDMSNET3-3.06.00	07/29/95
	NETASPI3.NLM	NETASPI-3.04.00	07/31/95
Netware v. 4.x	SDMSNET4.DSK	SDMSNET4-3.06.00	07/29/95
	NETASPI4.NLM	NETASPI-3.04.00	07/31/95
Unixware v. 1.x	UNIXWARE.Z	C8XX-3.00.00	02/17/95
Unixware v. 2.x	UW2X.DD	C8XX-3.00.00	03/20/95
NEXTSTEP 3.x	SYM53C8.CFG	NEXTSTEP-3.00.00	04/25/95

Current SYMBIOS LOGIC PCI SDMS Utilities:

Utility	Name	Version	Date
Low Level Format Utility	SCSIFMT.EXE	SCSIFMT-3.03.00	02/05/95

If the SCSI Boot-extension in the BIOS from DIGITAL-LOGIC AG does not support the environment used by the customer, then check for these drivers at NCR directly or at DIGITAL-LOGIC AG.

11 SOUNDPORT DRIVER INSTALLATION

Since boardversion V2.2, the sound chip is an ESS1869 and therefore, please refer always to all the ESS drivers and programs

The power- amplifier needs a +12V power supply.
Please be sure, that the +12V / 200mA is connected to the external main power input.

To download the latest chip producer drivers, go to:

http://www.esstech.com or http://www.digitallogic.com

11.1 DOS Driver

ESSCFG.EXE allows the user to configure the ESS sound chip with a base address, a DMA chanel, an IRQ channel, and an address for the MPU-401 port, if a wavetable is supported by the sound card.

ESSVOL.EXE allows the user to configure the output volume level of the mixer in the sound chip.

Type
ESSCFG.exe [Enter]
to run the program or
ESSCFG.EXE /? [Enter]
for help.

Type
ESSVOL.EXE [Enter]
to run the program or
ESSVOL.EXE /? [Enter]
for help.

Typical parameters are:
address : 220
DMA : 1
IRQ : 5
MPU-401 : 330

Procedure example

Run **esscfg.exe** and use the following settings:

IRQ	= 7
DMA	= 1
2nd DMA	= 0
Adr.	= 220

1) All other = disabled

2) Reboot the system

3) Add a VESA driver (**vesa.com**) to the **autoexec.bat**
(Necessary when using the shareware "SUPERSONIC" and if grafic controller is set to Vesa LocalBus)

4) Install des program SUPERSONIC with **install.exe** and configure the devices afterwards with the **setup.exe**
(When using the SBPRO driver, one can also record)

5) Add a mouse driver in the **autoexec.bat** if SUPERSONIC does not detect any

EXAMPLES:

AUTOEXEC.BAT

```
C:\SOUND\ESSCFG.EXE /A:220 /I:7 /D:1 /E:0 /B:D /J:E
@ECHO OFF
PROMPT $p$g
PATH C:\DOS;c:\ss;c:\sound;
SET TEMP=C:\DOS
MODE CON CODEPAGE PREPARE=((850) C:\DOS\EGA.CPI)
MODE CON CODEPAGE SELECT=850
KEYB SG,,C:\DOS\KEYBOARD.SYS
vesa.com
lmouse.com
```

CONFIG.SYS

```
DEVICE=C:\DOS\SETVER.EXE
DEVICE=C:\DOS\HIMEM.SYS /testmem:off
DOS=HIGH
COUNTRY=041,,C:\DOS\COUNTRY.SYS
DEVICE=C:\DOS\DISPLAY.SYS CON=(EGA,,1)
FILES=30
rem DEVICE=C:\SOUND\ES1868.COM /A:0 /I:0
```

11.2 WIN311, OS2, WIN95, WIN98, WIN NT

For all the other operating systems (OS), please run the setup program to install the appropriate drivers, if not already recognized by the OS.

Note, that depending on the BIOS, one has might to reserve certain IRQ's to avoid corruptions with other devices.

11.3 AD1816 sound chip

11.3.1 Driver for WIN 3.11

Insert the DRIVER DISK FOR WIN3.1, after starting windows V3.1. Run „SETUP.EXE“ on the driver floppy-disk A:. Choose „INSTALL“ for all the files to be loaded and system files to be modified. The setup utility allows a different directory to be choosen other than default „ C:\ADISOUND“ for copying. Select „CONTINUE“ to begin copying the files from the disk. After the setup has completed type „EXIT“, restart Windows. You may configure the device before restarting Windows by choosing „CONFIG“. This „AD1816 I/O Configuration“ allows the user to configure the device to something other than default.

After exiting setup, other configuration changes must be made using the program item drivers under AD1816 Control Panel !

In the Control Panel for the AD1816 the following setting may be made:

Windows Sound System:

Base Port:	Address 530 - 53fh	
IRQ	IRQ5	
DMA Play	DMA 01	
DMA Rec.	DMA 00	

MPU401:

Base Port:	Address 330-331h	
IRQ:	IRQ9	

Sound Blaster System:

Base Port:	220-22fh	

Others:

OPL3 Port:	388h-388h	
Game Port:	201h-201h	(not free on MSM-P5!)

After exiting setup and restarting Windows V3.1 the drivers will be loaded. If there is an I/O, DMA or IRQ conflict between the audio drivers and other devices in the system, use the Willow Pond Universal Sound-Comm Driver setup to change any setting, it is located in „drivers“ under Control Panel. The MPU-401 I/O address and IRQ settings are located in the Roland MPU-401 driver.

11.3.2 Driver for WIN 95

After installing the MSMM104 card, Win95 will recognize the new hardware by displaying a dialog box „New Hardware Found AD1816“. Insert DRIVER DISK WIN95 into the floppydisk A:. Select the option „Driver from disk provided by hardware manufacturer“, and hit ENTER. In the next windows select the default driver and hit OK. Select the default driver also for the GAMEPORT. The DRIVER DISK WIN95 must be in the floppy drive and the correct drivers are loaded. Remove the disk and restart the system when prompted. Your soundcard is now active.

11.3.3 Driver for NT4.0

After installing the MSMM104 card, NT will recognize the new hardware by displaying a dialog box saying „New Hardware Found AD1816“. Insert DRIVER DISK NT4.0 into the floppydisk A:. Select the option „Driver from disk provided by hardware manufacturer“, and hit ENTER. On the next windows select the default driver and hit OK. Select the default driver also for the GAMEPORT. The DRIVER DISK NT must be in the floppy drive and the correct drivers are loaded. Remove the disk and restart the system when prompted. Your soundcard is now active.

11.3.4 Bundled Applications, MediaRack

Insert the Disk witch contains all the bundled and optional applications.
Run a:\setup.exe (for Win 3.11, Win95, NT4.0).
The installer will create a program group called „bundled applications“ and „optional applications“.

Included applications:

- MEDIA RACK
- MEDIA LAUNCHER
- WAVE SHAPER
- DOC TALKER TTS and NOTE TALKER TTS
- KARAOKE PRODUCER
- PRESTO ARRANGER

12 INSTALLING THE FLASHDISK DOC2000

On the SSD 36pin socket a DiskOnChip DOC2000 module from M-Systems may be installed with a capacity of 512k to 12MByte. This device is available from DIGITAL-LOGIC AG.

Operating Systems:

DOS, DL-DOS, RTX-DOS, WIN 3.11, ROM-WIN are working with these drivers.
All other non DOS compatible systems need a driver.

Give attention to the pin 1 orientation in the 32pin SSD socket.

Latest drivers are available at http://www.m-sys.com

12.1 Enabling and Formatting of the DiskOnChip-Modules

Enabling:

No handlings need.

Format:

1. Boot up from the standard floppydisk A: or from a harddisk.

2. Enter the tooldisk from M-Systems containing the formattool DFORMAT.EXE

3. Start format utility
   The screen should inform about the status of the flashdisk.

4. Enter the DOS-Bootdisk and transfer the bootfiles with SYS A: C:
   From this moment, the flashdisk is now the bootable drive C: and if any harddisk is conencted it changes to letter D: and E:

13 BUILDING A SYSTEM

To build up a system based on your board, you should prepare the following equipments:

- A stable power supply of 5V (> 3 ampères), depending on the cpu, memory, etc.
- Assemble CPU with the proper clk- settings and cooling (fan) depending on board.
- If necessary, a 12V power supply for LCD or onboard sound.
- 8 ohm speaker for an executed beep code (if available on the board). One may use a capacity of 1µF connected to VCC depending on the board.
- A micro- floppy disk drive (3,5") with a PC floppy cable (26 pin) or a standard FDD with appropriate cable converter. You need at least one floppy to boot for the first time.
- A harddisk IDE 2,5" or 1,8" with the appropriate cable (44 pin and 2mm grid). Do not use a too long a cable to avoid accessing problem as the IDE controller is may not able to drive the HDD.
- Connect a LCD or a monitor.
- Use an AT-compatible keyboard (5 PC) or (6 PC {PS/2} with an appropriate adapter).
- If desired, connect a mouse to it (COM or PS/2 if usable on the board).
- Connect a battery (Lithium 3V or NiMH 3.6V depending on the board) to store the data in the BIOS.

13.1 Starting up the System

Power-up the system and wait for the BIOS to show the BIOS activity on the screen. The BIOS diagnoses the system and displays the size of the memory being tested. Note: you may can not bypass the memory test depending on the BIOS producer.

CMOS-SETUP

If the CMOS configuration is incorrect, the BIOS tells you to enter the setup screen by pressing a key. Select the correct options with the arrow keys and save them.

	AMI
BIOS setup	DEL
Change values	PgUp / PgDn
Jump	ARROWS
Save	F10
Back / exit	ESC

BEEP CODE:

AMI	
1 short	DRAM refresh
1 long	POST ok
1 cont.	Power supply
1 l / 1 s	Motherboard
1 l / 2 s	Graphic card
1 l / 3 s	Video DAC
2 s	Parity
2 l / 2 s	Video BIOS
3 s	Base 64k memory failure
3 s / 3 l / 3 s	Ram
4 s	Timer not operational
5 s	Prozessor error
6 s	8042 gate A20 failure
7 s	Prozessor exeption interrupt
8 s	Display memory read / write error
9 s	ROM checksum error
10 s	CMOS shutdown register read / write error
11 s	Cache error external cache bad

13.2 Error on boot time

A. If the display works:

1. Check if you have a bootable floppy or harddisk.
2. Check the CMOS parameter with the setup tools.
3. Reset the CMOS RAM with the reset jumper J27 on the board. Close Jumper J27 for 5 seconds until the power-on procedure. Remove the jumper and the system will start with BIOS-defaults.
4. Re-enter the correct values with Setup.

B. If no display on the screen is available:

1. Check the power circuitry.
2. Check the polarities of the cables.
3. Measure the voltage of the power supply under load and offload.
4. Measure the current between the supply and the MICROSPACE PC.
5. Connect a floppy: does the bezel led light blink?
6. Does the harddisk spindle motor start?
7. Reset the CMOS-RAM: see A.3.

C. If the error appears again

1. Contact your nearest Digital-Logic dealer for Technical Support.
2. Or contact our Technical Support by Fax ++41 32 681 53 31
   DIGITAL-LOGIC AG, Switzerland

14 DIAGNOSTICS

Check point Description

Uncompressed INIT code check-points

D0	NMI is Disabled. CPU ID saved. Init code Checksum verification starting.
D1	To do DMA init, Keyboard controller BAT test, start memory refresh and going to 4GB flat mode.
D3	To start Memory sizing.
D4	To come back to real mode. Execute OEM patch. Set stack.
D5	E000 ROM enabled. Init code is copied to segment 0 and control to be transfered to segment 0.
D6	Control is in segment 0. To check <CTRL><HOME> key and verify main BIOS checksum..
D7	Main BIOS runtime code is to be decompressed and control to be passed to main BIOS in shadow RAM.

Boot Block Recovery Code check-points

E0	Onboard Floppy Controller (if any) is initialized. To start base 512K memory test.
E1	To initialize interrupt vector table.
E2	To initialize DMA and interrupt controllers.
E6	To enable floppy and timer IRQ, enable internal cache.
ED	Initialize floppy drive.
EE	Start looking for a diskette in drive A: and read 1st sector of the dis kette.
EF	Floppy read error.
F0	Start searching 'AMIBOOT.ROM' file in root directory.
F1	'AMIBOOT.ROM' file not present in root directory.
F2	Start reading FAT table and analyse FAT to find the clusters occupied by 'AMIBOOT.ROM' file.
F3	Start reading 'AMIBOOT.ROM' file cluster by cluster.
F4	'AMIBOOT.ROM' file not of proper size.
F5	Disable internal cache.
FB	Detect Flash type present.
FC	Erase Flash.
FD	Program Flash.
FF	Flash program successful. BIOS is going to restart.

Runtime code is uncompressed in F000 shadow ram

03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable Cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS> , <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and IRQC
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15us ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization about to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different BUSes init (system, static, output devices) to start if present.
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace chec king.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate Display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power on message.
38	Different BUSes init (input, IPL, general devices) to start if present.
39	Display different BUSes initialization error messages. *(Please see Appendix for details of different BUSes.)*
3A	New cursor position read and saved. To display the Hit <DEL> message.

40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point No. 4Eh.)
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Goto check point No. 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for seq. and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written. Global data init done. To check for lock-key.
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different BUSes optional ROMs from C800 to start. *(Please see Appendix-I for details of different BUSes.)*
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is completed. Going to check extd keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	To uncompress DMI data and execute DMI POST init.
B0	System configuration is displayed.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

APPENDIX

The system BIOS gives control to the different BUSes at following check-points to performe various tasks on the different BUSes.

CHECK-POINT	DESCRIPTION OF CHECK-POINT
2A	Different BUSes init (system, static, output devices) to start if present.
38	Different BUSes init (input, IPL, general devices) to start if present.
39	Display different BUSes initialization error messages.
95	Init of different BUSes optional ROMs from C800 to start.

While control is inside the different BUS routines, additional check-points are output to port 80h as WORD to identify the routines under execution. These are WORD check-points, the LOW BYTE of check-point is the system BIOS check-point from where the control is passed to the different BUS routines and the HIGH BYTE of check-point is the indication of which routine is being executed in different BUSes. The details of HIGH BYTE of these check-points are as follows:

HIGH BYTE XY

the upper nibble 'X' indicates the function# is being executed. 'X' can be from 0 to 7.

0 = func#0, disable all devices on the BUS concerned.
1 = func#1, static devices init on the BUS concerned.
2 = func#2, output device init on the BUS concerned.
3 = func#3, input device init on the BUS concerned.
4 = func#4, IPL device init on the BUS concerned.
5 = func#5, general device init on the BUS concerned.
6 = func#6, error reporting for the BUS concerned.
7 = func#7, add-on ROM init for all BUSes.

the lower nibble 'Y' indicates the BUS on which the different routines are being executed. 'Y' can be from 0 to 5.

0 = Generic DIM (Device Initialization Manager).
1 = Onboard System devices.
2 = ISA devices.
3 = EISA devices.
4 = ISA PnP devices.
5 = PCI devices.

15 AMIBIOS® HIFLEX SETUP DESCRIPTION

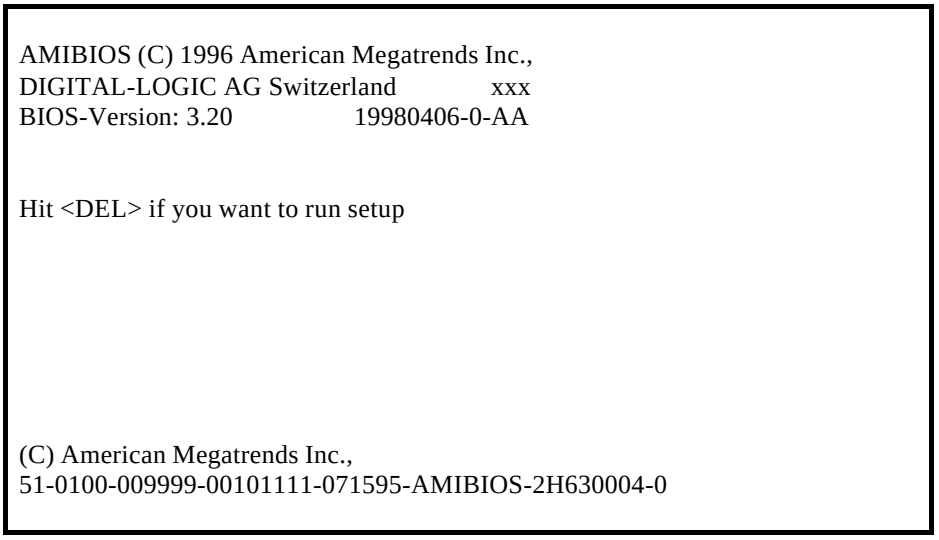
The system configuration information and chipset register information is stored in the CMOS RAM. This information is retained by a battery when the power is off. Enter the BIOS setup (if needed) to modify this information.

Below is the description on how to enter BIOS setup , and the meaning of each option.

15.1 Entering BIOS Setup

Enter the AMI® setup Program's Main Menu as follows:

1.Turn on or reboot the system. The following screen appears with a series of diagnostic check.



2.When the "Hit <DEL>“ message appears, press <DEL> key to enter the BIOS setup screen.

Note: *If you don’t want to modify CMOS original setting, don’t press any key; just wait for the system to boot up.*

3. After pressing <DEL> key, the BIOS Setup screen (as below) will display.

AMIBIOS HIFLEX SETUP UTILITY – VERSION 1.15 (C) 1996 American Megatrends, Inc. All Rights Reserved
Standard CMOS Setup Advanced CMOS Setup Advanced Chipset Setup Power Management Setup PCI / Plug and Play Setup Peripheral Setup Auto-Detect Hard Disks Change User Password Change Supervisor Password Change Language Setting Auto Configuration with Optimal Settings Auto Configuration with Fail Safe Settings Save Settings and Exit Exit without Saving
Standard CMOS Setup for changing time, date, hard disk type, etc. ESC : Exit - ¯: Sel F2/F3 : Color F10 : Save & Exit

4. Use the <- > and <¯> key to move the highlight scroll up or down.

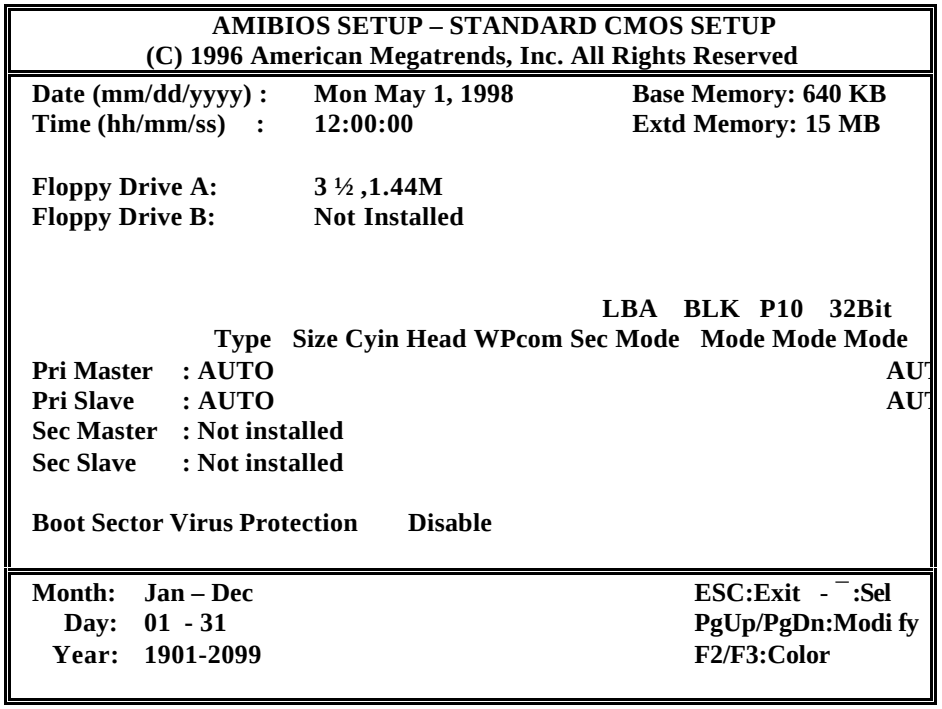
5. Use the <ENTER> key to choose the option.

6. To exit, press <ESC>. To save and exit, press <F10>.

7. Section 3-2 to 3-7 will describe the option in details.

15.2 Standard CMOS Setup

1. Press <ENTER> on "Standard CMOS Setup" of MAIN MENU SCREEN and the above screen appears.



2. Use <- > and <¯> to choose the item. Use <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with Standard CMOS Setup, press <Esc> to return to the main menu screen.

15.3 Advanced CMOS Setup

1. Press <ENTER> on "Advanced CMOS Setup" of MAIN MENU SCREEN and the screen as below will display.

AMIBIOS SETUP - ADVANCED CMOS SETUP (C)1996 American Megatrends, Inc. All Rights Reserved		
Quick Boot	**Enabled**	**Available Options:**
1st Boot Device	**Floppy**	**Disabled**
2nd Boot Device	**IDE-0**	**Enabled**
3rd Boot Device	**Disabled**	
4th Boot Device	**Disabled**	
Try Other Boot Devices	**Yes**	
S.M.A.R.T. for Hard Disks	**Disabled**	
BootUp Num-lock	**On**	
PS/2 Mouse Support	**Enabled**	
Typematic Rate	**Fast**	
System Keyboard	**Present**	
Primary Display	**VGA/EGA**	
Password Check	**Setup**	
Parity Check	**Disabled**	
Wait for 'F1' If Error	**Disabled**	
Hit 'DEL' Message Display	**Enabled**	
Internal Cache	**Writeback**	
External Cache	**Disabled**	
System BIOS Cacheable	**Enabled**	**ESC: Exit - ¯:: Sel**
C000,16k Shadow	**Enabled**	**PgUp/PgDn: Modify**
		F2/F3 : Color

2. Use <- > and <¯> to choose the item. Use <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with Advanced CMOS Setup, press <Esc> to return to the main menu screen.

15.3.1 A short description of this screen's items follows:

Quick Boot	Set this option to *Enabled* to permit the AMIBIOS to boot within 5 seconds. This option replaces the old **Above 1 MB Memory Test** option.
1st Boot Device	This option sets the sequence of boot drives that AMIBIOS attempts to boot from after AMIBIOS POST completes. The settings are *IDE-0 – IDE-3, FLOPPY, FLOPTICAL, CDROM, SCSI, NETWORK, Disabled.*
2nd-4th Boot Device	These options sets the sequence of boot drives after the first device. The settings are *FLOPPY, FLOPTICAL, CDROM, Disabled.*
Try Other Boot Devices	Set this option to *Yes* to instruct AMIBIOS to attempt to boot from any other drive in the system if it cannot find a boot drive among the drives specified in the **1st Boot Device**, **2nd Boot Device**, **3rd Boot Device**, and **4th Boot Device** options. The settings are *Yes* or *No*.
S.M.A.R.T. for Hard Disks	Set this option to *Enable* to permit the AMIBIOS to use the SMART (Self Monitoring Analysis and Reporting Technology) protocol for reporting server system information over a network. The settings are *Enabled* or *Disabled*.
BootUp Num-lock	Set this option to ON to turn the Num Lock key On at system boot. The settings are ON or OFF. The Optimal and Fail-Safe default settings are ON.
PS/2 Mouse Support	Set this option to *Enable* to enable AMIBIOS support for a PS/2-type mouse.

	The settings are *Enabled* or *Disabled*.
Typematic Rate	This option sets the rate at which characters displayed on the screen repeat when a key is pressed and held down. The settings are *Fast* or *Slow* characters per second.
System Keyboard	This option configures the keyboard. The settings are *Present* or *Absent*. If you select Absent, AMIBIOS does not report keyboard errors.
Primary Display	This option configures the primary display subsystem in the computer. The settings are *Absent*, *VGA/EGA*, *CGA40x25*, *CGA80x25* or *Mono (monochrom).*
Password Check	This option specifies the type of AMIBIOS password protection that is implemented. The settings are *Setup* or *Always*.
Parity Check	Set this option to *Enabled* to make sure that AMIBIOS checks the parity of all system memory. The settings are *Enabled* or *Disabled*.
Wait for 'F1' if Eror	If this options is set to Enabled, AMIBIOS waits for end user to press <F1> before continuing. If this option is set to Disabled, AMIBIOS continues the boot process without waiting for <F1> to be pressed. The settings are Enabled or Disabled.
Hit 'DEL' Message Display	Disabling this option prevents from appearing when the system boots. The settings are *Enabled* or *Disabled*.
Internal Cache	This option selects type of caching algorithm used by AMIBIOS and CPU for L1 cache memory (internal to the CPU). The settings are *WriteBack* or *Disabled*.
External Cache	This option selects type of caching algorithm used by AMIBIOS and CPU to acces L2 secondary (external) cache memory. The settings are *WriteBack*, *WriteThru* or *Disabled.*
System BIOS Cacheable	AMIBIOS always copies the system BIOS from ROM to RAM for faster execution. Set this option to Enabled to permit this contents of the F0000h RAM memory segment to be written to and read from cache memory. The settings are *Enabled* or *Disabled*.
C000,16k Shadow **C400,16k Shadow**	These options specify the contents of the video ROM at C0000h are handled. The settings are *Disabled*, *Cached* or *Enabled.*
C800,16k Shadow **CC00,16k,Shadow** **D000,16k Shadow** **D400,16k Shadow** **D800,16k Shadow** **DC00,16k Shadow**	These options specify how the contents of the adaptor ROM named in the option title are handled. The ROM area that is not used by ISA-BUS will be allocated to PCI-BUS. The settings are *Disabled*, *Cached* or *Enabled*.

15.4 Advanced Chipset Setup

1. Press <ENTER> on "Advanced Chipset Setup" of MAIN MENU SCREEN and the screen as below will display.

AMIBIOS SETUP - ADVANCED CHIPSET SETUP (C)1996 American Megatrends, Inc. All Rights Reserved		
Memory Hole	**Disabled**	**Available option:**
IRQ12/M Mouse Function	**Enabled**	**Disabled**
8Bit I/O Recovery Time (Sysclk)	**1**	**512-640K**
16Bit I/O Recovery Time (Sysclk)	**1**	**15-16M**
DRAM Timings	**60ns**	
Refresh Rate	**66MHz**	
Turbo Read LeadOff	**Disabled**	
Read Burst Timing	**x333**	
Write Burst Timing	**x333**	
Fast RAS to CAS Delay (Clocks)	**3**	
LeadOff Timing	**7/6/3/4**	
Turbo Read Pipelining	**Disabled**	
Speculative Leadoff	**Disabled**	
Turn-Around Insertion	**Disabled**	
Peer Concurrency	**Enabled**	
PCI 2.1 Passive Release Enable	**Enabled**	
Delayed Transaction enable	**Enable**	
		ESC:Exit - ¯:Sel **PgUp/PgDn:Modify** **F2/F3 : Color**

2. Use <- > and <¯> to choose the item. Use <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with Advanced Chipset Setup, press <Esc> to return to the main menu screen.

15.4.1 A Short description of the screen's items follows:

Memory Hole	This option allows the end user to specify the location of memory hole. The settings are *Disabled*, *512K-640K* or 15M-16M (from 15 MB ro 16 MB).
IRQ12/M Mouse Function	Set this option to *Enabled* to provide IRQ12 support for PS/2 Mouse. The settings are *Enabled* or *Disabled*.
8 Bit I/O Recovery Time	This option specifies the length of a delay inserted between consecutive 8-bit I/O operations. The settings are *Disabled*, *8*, *1* (Sysclk), *2*, *3*, *4*, *5* or *6*.
16 Bit I/O Recovery Time	This option specifies the length of a delay inserted between consecutive 16-bit I/O operations. The settings are *Disabled*, *4*, *1* (Sysclk), *2*, *3*, or *4*.
DRAM Timings	This option specifies the RAS Access Time parameter for the installed DRAM. The settings are *Manual*, *60ns* or *70ns*.
Peer Concurrency	Set this option to Enabled to enable PCI Concurrency. The settings are *Enabled* or *Disabled*.
PCI 2.1 Passive Release	Set this option to *Enabled* to enable PCI Passive Release. The settings are *Enabled* or *Disabled*.
Delayed Transaction enable	Set this option to *Enabled* to enable Delayed PCI R/W Transaction. The settings are *Enabled* or *Disabled*.

15.5 Power Management Setup

1. Press <ENTER> on "Power Management Setup" of MAIN MENU SCREEN and the screen (as below) will display.

AMIBIOS SETUP - POWER MANAGEMENT SETUP (C)1996 American Megatrends, Inc. All Rights Reserved		
Power Management/APM	**Disabled**	**Available Options:**
Instant-On Timeout (Minute)	**Disabled**	**Disable**
Green PC Monitor Power State	**Standby**	**Enabled**
Video Power Down Mode	**Standby**	**Inst-ON**
Hard Disk Power Down Mode	**Suspend**	
Hard Disk Time Out (Minute)	**Disabled**	
Standby Time Out (Minute)	**1**	
Suspend Time Out (Minute)	**1**	
Slow Clock Ratio 1:8		
IRQ3 Active (at suspend)	**Ignore**	
IRQ4 Active (at suspend)	**Ignore**	
IRQ5 Active (at suspend)	**Ignore**	
IRQ7 Active (at suspend)	**Ignore**	
IRQ8 Active (at suspend)	**Ignore**	
IRQ9 Active (at suspend)	**Ignore**	
IRQ10 Active (at suspend)	**Ignore**	
IRQ11 Active (at suspend)	**Ignore**	**ESC:Exit - ¯:SEL**
IRQ12 Active (at suspend)	**Both**	**PgUp/PgDn:Modify**
IRQ13 Active (at suspend)	**Ignore**	**F2/F3 : Color**
IRQ14 Active (at suspend)	**Monitor**	

2. Use <-> and <¯> to choose the item. Use <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with Power Management Setup, press <Esc> to return to the main menu screen.

15.5.1 A short description of this screen's items follows:

Power Management/APM	Set this option to Enable to enable the Intel Chipset power management features and APM (Advanced Power Management). The settings *are Enabled*, *Disabled* or *Inst-ON*.
Instant-On Timeout (Minute)	Set this option to Enabled to enable the AMIBIOS support for the Intel InstantOn feature. The settings are *Disabled* or *1-15*.
Green PC Monitor Power State	This option specify the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power savings state after the specified period of display inactivity has expired. The settings are *Off*, *Standby*, *Suspend* or *Disabled*.
Video Power Down Mode	This option specifies the power conserving state that the VESA VGA video subsystem enters after the specified period of display inactivity has expired. the settings are *Disabled*, *Standby* or *Suspend*.
Hard Disk Power Down Mode	This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. the settings are *Disabled*, *Standby* or *Suspend*.
Hard Disk Time Out (Minutes)	This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters power-conserving

	state specified in the **Hard Disk Power Down Mode** option (see the previous selection). The settings are *Disabled* or *1-14 min.*
Standby Timeout (Minutes)	This option specifies the length of a period of system inactivity while in Full power on state. When this length of time expires, the computer enters Standby power state. The settings are *Disabled* or *1-14 min*.
Suspend Timeout (Minutes)	This option specifies the length of a period of system inactivity while in Standby state. When this length of time expires, the computer enters Suspend power state. The settings are *Disabled* or *1-14 min*.
Slow Clock Ratio	This option specifies the speed at which clock runs in power saving states. The settings are expressed as a percentage of the standard clock speed. The settings are *1:1*, *1:2*, *1:4*, *1:8*, *1:16*, 1:32, *1:64* or *1:128*.
IRQ3/4/5/7/9/10/11/12/13/14 Active (at suspend)	When set to *Monitor*, these optins enable event monitoring on the specified hardware interrupt request line. If set to *Monitor* and the computer is in a power saving state, AMIBIOS watches for activity on the specified IRQ line. The computer enters the full on power state if any activity occurs. AMIBIOS reloads the Strandby and Suspend timeout timers if activity occurs on the specified IRQ line. No monitoring activity if the option is set to Ingore. The settings for each of these options are *Monitor*, *Ignore*, *Wakeup* or *Both*.

15.6 PCI / Plug and Play Setup

1. Press <ENTER> on "PCI/PLUG and PLAY Setup" of MAIN MENU SCREEN and the screen as below will display.

AMIBIOS SETUP - PCI/PLUG AND PLAY SETUP (C)1996 American Megatrends, Inc. All Rights Reserved		
Plug and Play Aware O/S	**No**	**Available Options**
PCI Latency Timer (PCI Clocks)	**64**	**No**
PCI IDE Busmaster	**Disabled**	**Yes**
DMA Channel 0	**PnP**	
DMA Channel 1	**PnP**	
DMA Channel 3	**PnP**	
DMA Channel 5	**PnP**	
DMA Channel 6	**PnP**	
DMA Channel 7	**PnP**	
IRQ3	**PCI/PnP**	
IRQ4	**PCI/PnP**	
IRQ5	**PCI/PnP**	
IRQ7	**PCI/PnP**	
IRQ9	**PCI/PnP**	**ESC:Exit - ¯:Sel** **PgUp/PgDn:Modify** **F2/F3 : Color**
IRQ10	**PCI/PnP**	
IRQ11	**PCI/PnP**	
IRQ14	**PCI/PnP**	
IRQ15	**PCI/PnP**	
Reserved Memory Size	**Disabled**	
Reserved Memory Address	**C8000**	

2. Use <-> and <¯> to choose the item. Use <PgUp>and <PgDn> keys to modify the highlighted item.

3. After you have finished with PCI/Plug and Play Setup, press <Esc> to return to the main menu screen.

15.6.1 A short description of this screen's items follows:

Plug and Play Aware O/S	Set this option to *Yes* if the operating system in this computer is aware of and follows the Plug and Play specification. Currently, only Windows 95/98 is PnP-aware. The settings are *Yes* or *No*.

PCI Latency Timer (PCI Clocks)	This option specifies the latency timings (in PCI clocks) for all PCI devices on the PCI bus. The settings are *32*, *64*, *128*, *160*, *192*, *224* or *248*.
PCI IDE Busmaster	Set this option to *Enabled* to specifiy that the IDE controller on the PCI local bus includes a bus mastering capability. The settings are *Enabled* or *Disabled*.
DMA Channel 0 - 7	These options specify if the named DMA channel is available for use on the ISA/EISA bus or for PnP (Plug and Play). The settings are *ISA/EISA* or *PnP*.
IRQ3, 4, 5, 7, 9, 10, 11, 14, 15	These options specifiy the bus that the specified IRQ line is used on. These options allow you to reserve IRQs for legacy ISA adapter cards. These options determine if AMIBIOS should remove an IRQ from the pool of available IRQs passed to devices that are configurable by reading the ESCD NVRAM. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an *ISA/EISA* settings to it. Onboard I/O are configured as *PCI/PnP*. IRQ14 and 15 will not be available if the onboard PCI DIE is enabled. If all IRQs are set to *ISA/EISA* and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ9 will still be available for PCI and PnP devices, because at least one IRQ must be available for PCI and PnP devices. The settings are *ISA/EISA* or *PCI/PnP*.
Reserved Memory Size	This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are *Disabled*, *16K*, *32K* or *64K*.
Reserved Memory Address	This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are *C000*, *C4000*, *C8000*, *CC000*, *D0000*, *D4000*, *D8000* or *DC000*.

15.7 Peripheral Setup

1. Press <ENTER> on "PCI/PLUG and PLAY Setup" and the screen as below will display.

AMIBIOS SETUP – PERIPHERAL SETUP (C) 1996 American Megatrends, Inc. All Rights Reserved		
OnBoard FDC	**Auto**	**Available Options:**
OnBoard Serial Port1	**Auto**	**Auto**
OnBoard Serial Port2	**Auto**	**Disabled**
OnBoard Parallel port	**Auto**	**Enabled**
Parallel Mode	**ECP**	
OnBoard IDE	**Primary**	
		ESC:Exit - ¯:Sel **PgUp/PgDn:Modify** **F2/F3 : Color**

2. Use <- > and <¯> to choose the item. Use <PgUp> and <PgDn> keys to modify the highlighted item.

3. After you have finished with PCI/Plug and Play Setup, press <Esc> to return to the main menu screen.

15.7.1 A short description of this screen's items follows:

OnBoard FDC	This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are *Auto (AMIBIOS automatically determines if the floppy conrtoller should be enabled)*, *Enabled* or *Disabled*.
OnBoard Serial Port1	This option specifies the base I/O port address of serial port 1. The settings are *Auto (AMIBIOS automatically determines the correct base I/O address)*, *Disabled*, *3F8h*, *2F8h*, *2E8h* or *3E8h*.
OnBoard Serial Port2	This option specifies the base I/O port address of serial port 1. The settings are *Auto (AMIBIOS automatically determines the correct base I/O address)*, *Disabled*, *3F8h*, *2F8h*, *2E8h* or *3E8h*.
OnBoard Parallel Port	This option specifies the base I/O port address of the parallel port on the motherboard. The settings are *Auto (AMIBIOS automatically determines the correct base I/O port address)*, *Disabled*, *378h*, *278h* or *3BCh*.
Parallel Port Mode	This option specifies the parallel port mode. The settings are *Normal*, *EPP* or *ECP*.
OnBoard IDE	This option specifies the channel used by the IDE conrtoller on the board. The settings are *Disabled*, *Primary*, *Secondary* or *Both*.

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