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POST CODES

During the POST on AT-compatibles and above, special signals are sent to I/O port 80H at the beginning of each test (XT-class machines don't issue POST codes, although some with compatible BIOSes do). Some computers may use a different port, such as 84 for the Compaq, or 378 (LPT1) for Olivettis. IBM PS/2s use 90 or 190 (20-286), whilst some EISA (Award) machines send them to 300H as well. Try 680 for Micro Channel. Those at 50h are chipset or custom platform specific, and you might find a few go to the parallel port (AT&T, NCR).

POST Diagnostic cards can display these POST codes, so you can check your PC's progress as it starts and hopefully diagnose errors when the POST stops, though a failure at any given location does not necessarily mean that part has the problem; it's meant to be a guidepost for further troubleshooting. In this chapter, some general instructions are given for a typical POST card, which were provided by Xetal Systems, together with some of the more obscure POST codes. Having obtained a code, identify the manufacturer of the chipset on the motherboard, then refer to the tables that follow. The POST checks at three levels, *Early*, *Late* and *System Initialisation*. Early POST failures are generally fatal and will produce a beep code, because the video will not be active; in fact, the last diagnostic during Early POST is usually on the video, so that Late failures can actually be seen. System Initialisation involves loading configuration from the CMOS, and failures will generate a text message. Consistent failures at that point indicate a bad battery backup. During the POST, all the devices on the machine are counted and given parameters within which to opperate. The responses are gathered together and compared against a previously calculated checksum as a further check of readiness.

Be aware that not all PCI POST cards allow all codes through the bridge.

Shutdown or Reset Commands

The Reset command stops the current operation and begins fetching instructions from the BIOS, as if the power has just been switched on. The Shutdown command, on the other hand, just forces the CPU to leave protected mode for real mode, so the system behaves differently after each one. Before issuing the shutdown command, the BIOS sets a value into the shutdown byte in the CMOS, which is checked after a reset, so the BIOS can branch to the relevant code and continue where it left off.

One of the problems with shutdown handling is that the POST must do some handling before anything else, immediately after power-on or system reset. The path between the CPU and the BIOS ROM, as well as basic control signals, has to be working before the POST gets to its first diagnostic test (usually the CPU register test), so some of the circuitry that the CPU test is supposed to check will be checked by the shutdown handling instead, and you will get no POST indication if a critical failure occurs.

Manufacturing Loop Jumper

The phrase *Check for Manufacturing Jumper* refers to one on the motherboard that makes the POST run in a continuous loop, so you can burn in a system, or use repetitive cycling to monitor a failing area with an oscilloscope or logic analyzer. It usually forces a reset, so the POST has to start from the beginning every time. Compaq used the shorted jumper to make the POST to jump to another ROM at E000 just after power-on, which could have diagnostic code in it. IBM and NCR used a germanium or silicon diode to short together the keyboard connector pins 1 (cathode, bar) and 2 (5-pin DIN) or 1 (anode, arrow) and 5 (6-pin mini-DIN), so the POST checks the keyboard controller to see if the jumper is there.

WHAT IS A POST DIAGNOSTIC CARD?

Note: Under no circumstances shall the publisher, author, any manufacturer of POST diagnostic cards, or their agents or distributors be held liable in any way for damages, including lost profits, lost savings, or other incidental or consequential damages arising out of the use of, or inability to use, any product designed to make POST diagnostic codes visible on your system.

A POST card is an operating system independent expansion card for use with any x86-based computer with a suitable expansion bus (although older cards are usually 8-bit, XT class machines do not generally issue POST codes). There may be conversion products for purely Micro Channel and PCI systems, depending on the manufacturer, but PCI versions suffer from some shortcomings. When you install a PCI and an ISA POST card into a system, the ISA card will report all the faults. The PCI one, on the other hand, reports only some or the later codes, that is, those issued after ISA initialisation. In some cases, they do not provide any codes at all (the culprits are actually the bridge circuits in the various motherboard chipsets rather than the design of the card, and is one reason why some motherboard vendors suggest that their boards be tested with an ISA video card, especially with corrupted CMOS settings or when flashing the BIOS).

In bus master mode, PCI slots can be addressed individually by North Bridge logic, so the North Bridge acts like a filter, allowing information only to certain PCI slots. The same applies to IRQ lines in PCI designs; the IRQ lines are not bussed or are only bussed between selected PCI slots. The backwards compatibility to the legacy PC architecture is established through a routing table (a lookup table) via the BIOS, chipset and PCI Steering logic. This table differs for each particular design and/or chipset. According to the PCI standard, the 4 PCI interrupts can hardwired in various ways. The preferred/ideal way would be to have the 4 Interrupt lines from every PCI slot go to an Interrupt router.

Also allowed by the PCI bus specification is a more low end approach where the IRQ lines are bussed (all INTA# pins on every slot are bussed to an INTA# input on the Interrupt Router etc.). The resulting 4 lines would be routed to the classical IRQs #9 through #12.

Unfortunately, the ISA slots, together with the BIOS that generates the POST codes, connect to the South Bridge in the chipset, so a defective motherboard or system with corrupted CMOS settings may be unable to send information to the PCI bus anyway. In addition, with no ISA bus there is no universal diagnostic port. For example, some high end motherboards

by Epox and ASUS come with built in POST code displays or have a proprietary ports which need a special display unit.

Obtaining Information About Your Computer

At least the BIOS ROM's manufacturer and firmware revision number should be known, so you can check the codes in the following pages (see the front of the book for BIOS IDs). The manufacturing port or POST port should also be known.

ACER

Based on Award BIOS 3.03, but not exactly the same. Port 80h.

Code	Meaning	Code	Meaning
04	Start	4C	Shutdown 3
08	Shutdown	50	Shutdown 2
0C	Test BIOS ROM checksum	54	Shutdown 7
10	Test CMOS shutdown byte	55	Shutdown 6
14	Test DMA controller	5C	Test keyboard and auxiliarv I/O
18	Initialise system timer	60	Set up BIOS interrupt routines
1C	Test memory refresh	64	Test real time clock
1E	Determine memory type	68	Test diskette
20	Test 128K memory	6C	Test hard disk
24	Test 8042 keyboard controller	70	Test parallel port
28	Test CPU descriptor instruction	74	Test serial port
2C	Set up and test 8259 controller	78	Set time of day
30	Set up memory interrupts	7C	Scan for and invoke option ROMs
34	Set interrupt vectors and routines	80	Determine presence of math copro
38	Test CMOS RAM	84	initialize keyboard
3C	Determine memory size	88	Initialise svstem 1
XX	Shut down 8 (system halt C0h + checkpoint)	8C	Initialize system 2
40	Shutdown 1	90	Invoke INT 19 to boot OS
44	Initialise Video BIOS ROM	94	Shutdown 5
45	Set up and test RAM BIOS	98	Shutdown A
46	Test cache and controller	9C	Shutdown B
48	Test memory		

ALR

See also *Phoenix*.

Code	Meaning
01	80[3,4]86 register test in progress
02	Real-time clock write/read failure
03	ROM BIOS Checksum failure
04	Programmable Internal Timer Failure (or no video card)
05	DMA initialization failure
06	DMA page register write/read failure
08	RAM refresh verification failure
09	1st 64-KB RAM test in progress
0A	1st 64-KB RAM chip or data line multi-bit
0B	1st 64-KB RAM odd/even logic failure
0C	Address line failure 1st 64 KB RAM
0D	Parity failure 1st 64-KB RAM
10	Bit 01st 64-KB RAM failure
11	Bit 11st 64-KB RAM failure
12	Bit 2 1st 64-KB RAM failure
13	Bit 3 1st 64-KB RAM failure
14	Bit 4 1st 64-KB RAM failure
15	Bit 5 1st 64-KB RAM failure
16	Bit 6 1st 64-KB RAM failure
17	Bit 7 1st 64-KB RAM failure
18	Bit 8 1st 64-KB RAM failure
19	Bit 9 1st 64-KB RAM failure
1A	Bit A 1st 64-KB RAM failure
1B	Bit B 1st 64-KB RAM failure
1C	Bit C 1st 64-KB RAM failure
1D	Bit D 1st 64-KB RAM failure
1E	Bit E 1st 64-KB RAM failure
1F	Bit F 1st 64-KB RAM failure
20	Slave DMA register failure
21	Master DMA register failure
22	Master interrupt mask register failure
23	Slave interrupt mask register failure
25	Interrupt vector loading in progress
27	Keyboard controller test failure
28	Real-time clock power failure and checksum calculation in progress
29	Real-time clock configuration validation in progress
2B	Screen memory test failure
2C	Screen initialization failure
2D	Screen retrace test failure
2E	Search for video ROM in Progress
30	Screen believed operational-screen believed running with video ROM
31	Mono display believed operable
32	Colour display (40 column) believed operable
33	Colour display (80 column) believed operable

AMBRA

See *Phoenix*.

AMI

Not all tests are performed by all AMI BIOSes. These refer to 2 Feb 91 BIOS.

POST Procedures

Procedure	Explanation
NMI Disable	NMI interrupt line to the CPU is disabled by setting bit 7 I/O port 70h (CMOS).
Power On Delay	Once keyboard controller gets power, it sets hard and soft reset bits. Check keyboard controller or clock generator.
Initialise Chipsets	Check the BIOS, CLOCK or chipsets.
Reset Determination	The BIOS reads bits in the keyboard controller to see if hard or soft reset is required (soft will not test mem above 64K). Failure could be BIOS or keyboard controller.
ROM BIOS Checksum	BIOS performs a checksum on itself and adds a preset factory value to make it equal 00. Failure is due to the BIOS chips.
Keyboard Test	A command is sent to the 8042 (keyboard controller) which performs a test and sets a buffer space for commands. After the buffer is defined the BIOS sends a command byte, writes data to the buffer, checks the high order bits (Pin 23) of the internal keyboard controller and issues a No Operation (NOP) command.
CMOS	Shutdown byte in CMOS RAM offset 0F is tested, the BIOS checksum calculated and diagnostic byte (0E) updated before the CMOS RAM area is initialised and updated for date and time. Check RTC/CMOS chip or battery.
8237/8259 Disable	DMA and PIC are disabled before POST proceeds. Check the 8237 or 8259 chips.
Video Disable	Vvideo controller is disabled and Port B initialised. Check adapter if problems here.
Chipset Init/ Memory Detect	Memory addressed in 64K blocks; failure would be in chipset. If all memory is not seen, failure could be in a chip in the block after the last one seen.
PIT test	The timing functions of the 8254 interrupt timer are tested. The PIT or RTC chips normally cause problems here.
Memory Refresh	PIT's ability to refresh memory tested (if an XT, DMA controller #1 handles this). Failure is normally the PIT (8254) in ATs or the 8237 (DMA #1) in XTs.
Address Lines	Test the address lines to the first 64K of RAM. An address line failure.
Base 64K	Data patterns are written to the first 64K, unless there is a bad RAM chip in which case you will get a failure.
Chipset Init	The PIT, PIC and DMA controllers are enabled.
Set Interrupt Table	Interrupt vector table used by PIC is installed in low memory, the first 2K.
8042 check	The BIOS reads the buffer area of the keyboard controller I/O port 60.
Video Tests	Ttype of video adapter is checked for then tests are done on adapter and monitor.
BIOS Data Area	The vector table is checked for proper operation and video memory verified before protected mode tests are entered into. This is done so that any errors found are displayed on the monitor.
Protected Mode Tests	Do reads and writes to mem below 1 Mb. Failures are bad RAM, 8042 or data line.
DMA Chips	The DMA registers are tested using a data pattern.
Final Initialisation	These differ with each version. Typically, floppy and hard drives are tested and initialised, and a check made for serial and parallel devices. Information is compared against the CMOS, and you will see the results of any failures on the monitor.
Boot	The BIOS hands over control to the Int 19 bootloader; this is where you would see error messages such as non-system disk.

AMI BIOS 2.2x

Code	Meaning	Code	Meaning
00	Flag test	5A	Verify LAR instruction
03	Register test	5D	Verify VERR instruction
06	System hardware initialisation	60	Address line 20 test
09	BIOS ROM checksum	63	Unexpected exception test
0C	Page register test	66	Start third protected mode test
0F	8254 timer test	69	Address line test
12	Memory refresh initialisation	6C	System memory test
15	8237 DMA controller test	6F	Shadow memory test
18	8237 DMA initialisation	72	Extended memory test
1B	8259 interrupt controller initialisation	75	Verify memory configuration
1E	8259 interrupt controller test	78	Display configuration error messages
21	Memory refresh test	7B	Copy system BIOS to shadow memory
24	Base 64K address test	7E	8254 clock test
27	Base 64K memory test	81	MC 146818 real time clock test
2A	8742 keyboard self test	84	Keyboard test
2D	MC 146818 CMOS test	87	Determine keyboard type
30	Start first protected mode test	8A	Stuck key test
33	Memory sizing test	8D	Initialise hardware interrupt vector
36	First protected mode test	90	Math coprocessor test
39	First protected mode test failed	93	Determine COM ports available
3C	CPU speed calculation	96	Determine LPT ports available
3F	Read 8742 hardware switches	99	Initialise BIOS data area
42	Initialise interrupt vector area	9C	Fixed/Floppy controller test
45	Verify CMOS configuration	9F	Floppy disk test
48	Test and initialise video system	A2	Fixed disk test
4B	Unexpected interrupt test	A5	External ROM scan
4E	Start second protected mode test	A8	System key lock test
51	Verify LDT instruction	AE	F1 error message test
54	Verify TR instruction	AF	System boot initialisation
57	Verify LSL instruction	B1	Interrupt 19 boot loader

AMI Colour BIOS

Code	Meaning	Code	Meaning
00	Control to Int 19 boot loader	4C	Clear extended memory locations
01	CPU flag test	4D	Update CMOS memory size
02	Power-on delay	4E	Base RAM size displayed
03	Chipset initialization	4F	Memory Read/Write test on 640K
04	Soft/hard reset	50	Update CMOS on RAM size
05	ROM enable	51	Extended memory tested
06	BIOS ROM checksum	52	Re-size extended memory
07	8042 keyboard controller tested	53	Return CPU to real mode
08	8042 keyboard controller tested	54	Restore CPU registers
09	8042 keyboard controller tested	55	A-20 gate disabled
0A	8042 keyboard controller tested	56	BIOS vector recheck
0B	8042 keyboard controller tested	57	BIOS vector check complete

Code	Meaning	Code	Meaning
0C	8042 keyboard controller tested	58	Clear BIOS display setup message
0D	8042 keyboard controller tested	59	DMA, PIT tested
0E	CMOS checksum tested	60	DMA page register tested
0F	CMOS initialization	61	DMA #1 tested
10	CMOS/RTC status OK	62	DMA #2 tested
11	DMA/PIC disable	63	BIOS data area check
12	DMA/PIC initialization	64	BIOS data area checked
13	Chipset/memory initialization	65	Initialize DMA chips
14	8254 PIT timer tested	66	8259 PIC initialization
15	8254 PIT channel 2 timer tested	67	Keyboard tested
16	8254 PIT channel 1 timer tested	80	Keyboard reset
17	8254 PIT channel 0 timer tested	81	Stuck key and batch test
18	Memory refresh test (PIC)	82	8042 keyboard controller tested
19	Memory refresh test (PIC)	83	Lock key check
1A	Check 15-microsecond refresh (PIT)	84	Compare memory size with CMOS
1B	Check 30-microsecond refresh (PIT)	85	Password/soft error check
20	Base 64K memory tested	86	XCMOS/CMOS equipment check
21	Base 64K memory parity tested	87	CMOS setup entered
22	Memory Read/Write	88	Reinitialize chipset
23	BIOS vector table initialization	89	Display power-on message
24	BIOS vector table initialization	8A	Display wait and mouse check
25	Turbo check 8042 keyboard controller	8B	Shadow any option ROMs
26	Global data table for kb controller; turbo	8C	Initialize XCMOS settings
27	Video mode tested	8D	Reset hard/floppy drives
28	Monochrome tested	8E	Floppy compare to CMOS
29	Color (CGA) tested	8F	Floppy disk controller initialization
2A	Parity-enable tested	90	Hard disk compare to CMOS
2B	Optional system ROMs check start	91	Hard disk controller initialization
2C	Video ROM check	92	BIOS data table check
2D	Reinitialize main chipset	93	BIOS data check hat halfway
2E	Video memory tested	94	Set memory size
2F	Video memory tested	95	Verify display memory
30	Video adapter tested	96	Clear all Interrupts
31	Alternate video adapter tested	97	Optional ROMs check
32	Alternate video adapter tested	98	Clear all Interrupts
33	Video mode tested	99	Setup timer data/RS232 base
34	Video mode tested	9A	RS232 test; Locate and test serial ports
35	Initialize BIOS ROM data area	9B	Clear all Interrupts
36	Power-on message display	9C	NPU test
37	Power-on message display	9D	Clear all Interrupts
38	Read cursor position	9E	Extended keyboard check
39	Display cursor reference	9F	Set numlock
3A	Display BIOS setup message	A0	Keyboard reset
40	Start protected mode tested	A1	Cache memory test
41	Build mode entry	A2	Display any soft errors
42	CPU enters protected mode	A3	Set typematic rate
43	Protected mode Interrupt enable	A4	Set memory wait states
44	Check descriptor tables	A5	Clear screen
45	Check memory size	A6	Enable parity/NMI

Code	Meaning	Code	Meaning
46	Memory Read/Write tested	A7	Clear all Interrupts
47	Base 640K memory tested	A8	Control to ROM at E0000
48	Check 640K memory size	A9	Clear all Interrupts
49	Check extended memory size	AA	Display configuration
4A	Verify CMOS extended memory	00	Interrupt 19 boot loader
4B	Check for soft/hard reset		

AMI Ez-Flex BIOS

Code	Meaning	Code	Meaning
01	NMI disabled; Start CPU flag test	4C	Memory above 1MB cleared for soft reset
02	Power-on delay	4D	Update CMOS memory size
03	Chipset initialization	4E	Base RAM size displayed
04	Check keyboard for soft/hard reset	4F	Memory Read/Write test on 640K
05	ROM enable	50	Update CMOS on RAM size
06	BIOS ROM checksum	51	Extended memory tested
07	8042 keyboard controller tested	52	System is prepared for real mode
08	8042 keyboard controller tested	53	Return CPU to real mode
09	8042 keyboard controller tested	54	Restore CPU registers
0A	8042 keyboard controller tested	55	A-20 gate disabled
0B	8042 protected mode tested	56	BIOS data area rechecked
0C	8042 keyboard controller tested	57	BIOS data area recheckcomplete
0D	CMOS RAM shutdown register tested	58	Display setup message
0E	CMOS checksum tested	59	DMA register page tested
0F	CMOS initialization	60	DMA page register tested
10	CMOS/RTC status OK	61	DMA #1 tested
11	DMA/PIC disable	62	DMA #2 tested
12	Video display disabled	63	BIOS data area check
13	Chipset/memory initialization	64	BIOS data area checked
14	8254 PIT timer tested	65	Initialize DMA chips
15	8254 PIT channel 2 timer tested	66	8259 PIC initialization
16	8254 PIT channel 1 timer tested	67	Keyboard tested
17	8254 PIT channel 0 timer tested	80	Keyboard reset
18	Memory refresh test (PIT)	81	Stuck key and batch test
19	Memory refresh test (PIT)	82	8042 keyboard controller tested
1A	Check 15-microsecond refresh (PIT)	83	Lock key check
1B	Base 64K memory tested	84	Compare memory size with CMOS
20	Address lines tested	85	Password/soft error check
21	Base 64K memory parity tested	86	CMOS equipment check
22	Memory Read/Write	87	CMOS setup entered if selected
23	Perform setups before init vector table	88	Main chipset reinitialized after CMOS setup
24	BIOS vector table initialization	89	Display power-on message
25	8042 keyboard controller tested	8A	Display wait and mouse check
26	Global data table for kb controller	8B	Shadow any option ROMs
27	Perform setups for vector table initialization	8C	Initialize CMOS settings
28	Monochrome tested	8D	Reset hard/floppy drives
29	Color (CGA) tested	8E	Floppy compare to CMOS
2A	Parity-enable tested	8F	Floppy disk controller initialization

Code	Meaning	Code	Meaning
2B	Optional system ROMs check start	90	Hard disk compare to CMOS
2C	Video ROM check	91	Hard disk controller initialization
2D	Determine if EGA/VGA is installed	92	BIOS data table check
2E	Video memory tested	93	BIOS data table check complete
2F	Video memory tested	94	Set memory size
30	Video adapter tested	95	Verify display memory
31	Alternate video adapter tested	96	Clear all Interrupts
32	Alternate video adapter tested	97	Optional ROMs checked
33	Video mode tested	98	Clear all Interrupts
34	Video mode tested	99	Timer data setup
35	Initialize BIOS ROM data area	9A	RS232 test; Locate and test serial ports
36	Power on display cursor set	9B	Clear all Interrupts
37	Power-on message display	9C	Math coprocessor checked
38	Read cursor position	9D	Clear all Interrupts
39	Display cursor reference	9E	Extended keyboard check
3A	Display BIOS setup message	9F	Set numlock
40	Protected mode tested	A0	Keyboard reset
41	Build descriptor tables	A1	Cache memory test
42	CPU enters protected mode	A2	Display any soft errors
43	Protected mode Interrupt enable	A3	Set typematic rate
44	Check descriptor tables	A4	Set memory wait states
45	Check memory size	A5	Clear screen
46	Memory Read/Write tested	A6	Enable parity/NMI
47	Base 640K memory tested	A7	Clear all Interrupts
48	Memory below 1MB checked for soft reset	A8	Control to ROM at E0000
49	Memory above 1MB checked for soft reset	A9	Clear all Interrupts
4A	ROM BIOS data area checked	AA	Display configuration
4B	Memory below 1MB cleared for soft reset	00	Interrupt 19 boot loader

AMI Old BIOS; 08/15/88-04/08/90

Code	Meaning	Code	Meaning
01	NMI disabled & 286 reg. test about to start	3E	About to go to real mode (shutdown)
02	286 register test over	3F	Shutdown successful, entered in real mode
03	ROM checksum OK	40	About to disable gate A-20 address line
04	8259 initialization OK	41	Gate A-20 line disabled successfully
05	CMOS pending interrupt disabled	42	About to start DMA controller test
06	Video disabled & system timer counting OK	4E	Address line test OK
07	CH-2 of 8253 test OK	4F	Processor in real mode after shutdown
08	CH-2 delta count test OK	50	DMA page register test OK
09	CH-1 delta count test OK	51	DMA unit-1 base register test about to start
0A	CH-0 delta count test OK	52	DMA unit-1 channel OK; to begin CH-2
0B	Parity status cleared	53	DMA CH-2 base register test OK
0C	Refresh & system timer OK	54	About to test f/f latch for unit-1
0D	Refresh link toggling OK	55	f/f latch test both unit OK
0E	Refresh period ON/OFF 50% OK	56	DMA unit 1 & 2 programmed OK
10	Confirmed refresh ON, starting 64K memory	57	8259 initialization over
11	Address line test OK	58	8259 mask register check OK

Code	Meaning	Code	Meaning
12	64K base memory test OK	59	Master 8259 mask register OK; start slave
13	Interrupt vectors initialized	5A	To check timer, keyboard interrupt level
14	8042 keyboard controller test OK	5B	Timer interrupt OK
15	CMOS read/write test OK	5C	About to test keyboard interrupt
16	CMOS checksum/battery check OK	5D	Timer/keyboard interrupt not proper level
17	Monochrome mode set OK	5E	8259 interrupt controller error
18	Colour mode set OK	5F	8259 interrupt controller test OK
19	About to look for optional video ROM	70	Start of keyboard test
1A	Optional video ROM control OK	71	Keyboard BAT test OK
1B	Display memory read/write test OK	72	Keyboard test OK
1C	Alt display memory read/write test OK	73	Keyboard global data initialization OK
1D	Video retrace check OK	74	Floppy setup about to start
1E	Global equipment byte set for video OK	75	Floppy setup OK
1F	Mode set call for Mono/Colour OK	76	Hard disk setup about to start
20	Video test OK	77	Hard disk setup OK
21	Video display OK	79	About to initialize timer data area
22	Power on message display OK	7A	Verify CMOS battery power
30	Virtual mode memory test about to begin	7B	CMOS battery verification done
31	Virtual mode memory test started	7D	About to analyze diag results for memory
32	Processor in virtual mode	7E	CMOS memory size update OK
33	Memory address line test in progress	7F	About to check optional ROM C000:0
34	Memory address line test in progress	80	Keyboard sensed to enable setup
35	Memory below 1MB calculated	81	Optional ROM control OK
36	Memory size computation OK	82	Printer global data initialization OK
37	Memory test in progress	83	RS-232 global data initialization OK
38	Memory initialization over below 1MB	84	80287 check/test OK
39	Memory initialization over above 1MB	85	About to display soft error message
3A	Display memory size	86	Give control to system ROM E000:0
3B	About to start below 1MB memory test	87	System ROM E000:0 check over
3C	Memory test below 1MB OK	00	Control given to Int-19; boot loader
3D	Memory test above 1MB OK		

AMI Plus BIOS

Code	Meaning	Code	Meaning
01	NMI disabled (Bit 7 of I/O port 70h)	3E	About to go to real mode (shutdown)
02	286 register test over	3F	Shutdown successful, entered in real mode
03	ROM checksum OK	40	About to disable gate A-20 address line
04	8259 initialization OK	41	Gate A-20 line disabled successfully
05	CMOS pending interrupt disabled	42	About to start DMA controller test
06	System timer (PIT) counting OK	4E	Address line test OK
07	Channel 0 of 8259 PIC test OK	4F	Processor in real mode after shutdown
08	DMA CH-2 delta count test OK	50	DMA page register test OK
09	DMA CH-1 delta count test OK	51	DMA unit-1 base register test about to start
0A	DMA CH-0 delta count test OK	52	DMA 1 channel OK; about to begin CH-2
0B	Parity status cleared (DMA/PIT)	53	DMA CH-2 base register test OK
0C	Refresh & system timer OK (DMA/PIT)	54	About to test both units OK
0D	Refresh link toggling OK (DMA/PIT)	55	f/f latch test both unit OK

Code	Meaning	Code	Meaning
0E	Refresh period ON/OFF 50% OK	56	DMA unit 1 & 2 programmed OK
10	About to start 64K memory	57	8259 initialization over
11	Address line test OK	58	8259 mask register check OK
12	64K base memory test OK	59	Master 8259 mask register OK
13	Interrupt vectors initialized	5A	Check timer, keyboard interrupt level
14	8042 keyboard controller test OK	5B	Timer interrupt OK
15	CMOS read/write test OK	5C	About to test keyboard interrupt
16	CMOS checksum/battery check OK	5D	Timer/keyboard interrupt not in proper level
17	Monochrome mode set OK	5E	8259 interrupt controller error
18	Colour mode set OK	5F	8259 interrupt controller test OK
19	Video ROM Search	70	Start of keyboard test
1A	Optional video ROM control OK	71	Keyboard test OK
1B	Display memory read/write test OK	72	Keyboard test OK
1C	Alternate display memory OK	73	Keyboard global data initialization OK
1D	Video retrace check OK	74	Floppy setup about to start
1E	Global equipment byte set for video OK	75	Floppy setup OK
1F	Mode set call for Mono/Colour OK	76	Hard disk setup about to start
20	Video test OK	77	Hard disk setup OK
21	Video display OK	79	About to initialize timer data area
22	Power on message display OK	7A	Verify CMOS battery power
30	Virtual mode memory test about to begin	7B	CMOS battery verification done
31	Virtual mode memory test started	7D	Analyze diag test results for memory
32	Processor in virtual mode	7E	CMOS memory size update OK
33	Memory address line test in progress	7F	About to check optional ROM C000:0
34	Memory address line test in progress	80	Keyboard sensed to enable setup
35	Memory below 1MB calculated	81	Optional ROM control OK
36	Memory size computation OK	82	Printer global data initialization OK
37	Memory test in progress	83	RS-232 global data initialization OK
38	Memory initialization over below 1MB	84	80287 check/test OK
39	Memory initialization over above 1MB	85	About to display soft error message
3A	Display memory size	86	Give control to system ROM E000:0
3B	About to start below 1MB memory test	87	System ROM E000:0 check over
3C	Memory test below 1MB OK	00	Control given to Int-19; boot loader
3D	Memory test above 1MB OK		

AMI BIOS 04/09/90-02/01/91

Code	Meaning
01	NMI disabled and 286 register test about to start.
02	286 register test passed.
03	ROM BIOS checksum (32K at F800:0) passed.
04	Keyboard controller test with and without mouse passed.
05	Chipset initialization over; DMA and Interrupt controller disabled.
06	Video disabled and system timer test begin.
07	CH-2 of 8254 initialization half way.
08	CH-2 of timer initialization over.
09	CH-1 of timer initialization over.
0A	CH-0 of timer initialization over.

Code	Meaning
0B	Refresh started.
0C	System timer started.
0D	Refresh link toggling passed.
10	Refresh on and about to start 64K base memory test.
11	Address line test passed.
12	64K base memory test passed.
15	Interrupt vectors initialized.
17	Monochrome mode set.
18	Colour mode set.
19	About to look for optional video ROM at C000 and give control to ROM if present.
1A	Return from optional video ROM.
1B	Shadow RAM enable/disable completed.
1C	Display memory read/write test for main display as in CMOS setup program over.
1D	Display memory read/write test for alternate display complete if main display memory test returns error.
1E	Global equipment byte set for proper display type.
1F	Video mode set call for mono/colour begins.
20	Video mode set completed.
21	ROM type 27256 verified.
23	Power on message displayed.
30	Virtual mode memory test about to begin.
31	Virtual mode memory test started.
32	Processor executing in virtual mode.
33	Memory address line test in progress.
34	Memory address line test in progress.
35	Memory below 1MB calculated.
36	Memory above 1MB calculated.
37	Memory test about to start.
38	Memory below 1MB initialized.
39	Memory above 1MB initialized.
3A	Memory size display initiated-updated when BIOS goes through memory test.
3B	About to start below 1MB memory test.
3C	Memory test below 1MB completed; about to start above 1MB test.
3D	Memory test above 1MB completed.
3E	About to go to real mode (shutdown).
3F	Shutdown successful and processor in real mode.
40	Cache memory on and about to disable A20 address line.
41	A20 address line disable successful.
42	486 internal cache turned on.
43	About to start DMA controller test.
50	DMA page register test complete.
51	DMA unit-1 base register test about to start.
52	DMA unit-1 base register test complete.
53	DMA unit-2 base register test complete.
54	About to check F/F latch for unit-1 and unit-2.
55	F/F latch for both units checked.
56	DMA unit 1 and 2 programming over; about to initialize 8259 interrupt controller.
57	8259 initialization over.
70	About to start keyboard test.
71	Keyboard controller BAT test over.

Code	Meaning
72	Keyboard interface test over; mouse interface test started.
73	Global data initialization for keyboard/mouse over.
74	Display 'SETUP' prompt and about to start floppy setup.
75	Floppy setup over.
76	Hard disk setup about to start.
77	Hard disk setup over.
79	About to initialize timer data area.
7A	Timer data initialized and about to verify CMOS battery power.
7B	CMOS battery verification over.
7D	About to analyze POST results.
7E	CMOS memory size updated.
7F	Look for <DEL> key and get into CMOS setup if found.
80	About to give control to optional ROM in segment C800 to DE00.
81	Optional ROM control over.
82	Check for printer ports and put the addresses in global data area.
83	Check for RS232 ports and put the addresses in global data area.
84	Coprocessor detection over.
85	About to display soft error messages.
86	About to give control to system ROM at segment E000.
00	System ROM control at E000 over now give control to Int 19h boot loader.

AMI New BIOS; 02/02/91-12/12/91

Code	Meaning
01	Processor register test about to start and NMI to be disabled.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete. Any initialization before keyboard BAT is in progress.
04	Init before keyboard BAT complete. Reading keyboard SYS bit to check soft reset/ power-on.
05	Soft reset/ power-on determined. Going to enable ROM. i. e. disable shadow RAM/Cache.
06	ROM enabled. Calculating BIOS checksum, waiting for KB controller input buffer to be free.
07	ROM Checksum passed. KB controller I/B free. Issuing BAT comd to kboard controller.
08	BAT command to keyboard controller issued. Going to verify BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code issued. Going to write command byte data.
0B	Keyboard controller command byte written. Issuing Pin-23 & 24 blocking/unblocking command
0C	Pin 23 & 24 of keyboard controller is blocked/unblocked. NOP command to be issued next.
0D	NOP command processing done. CMOS shutdown register test to be done next.
0E	CMOS shutdown register R/W test passed. Calculating CMOS checksum, update DIAG byte.
0F	CMOS checksum calc done DIAG byte written. CMOS init. begins (If INIT CMOS IN EVERY BOOT is set).
10	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
11	CMOS Status register initialised. Going to disable DMA and Interrupt controllers.
12	DMA Controller #1 & #2, interrupt controller #1 & #2 disabled. Disable Video display and init port-B.
13	Video display disabled and port-B initialized. Chipset init/auto mem detection about to begin.
14	Chipset initialization/auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be complete.
16	Ch-2 timer test over. 8254 CH-1 timer test to be complete.
17	CH-1 timer test over. 8254 CH-0 timer test to be complete.
18	CH-0 timer test over. About to start memory refresh.

Code	Meaning
19	Memory Refresh started. Memory Refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 microsecond ON/OFF time.
1B	Memory Refresh period 30 microsec test complete. Base 64K memory test about to start.
20	Base 64k memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64k sequential data R/W test passed. Setup before Interrupt vector init about to start.
24	Setup before vector init complete. Interrupt vector initialization about to begin.
25	Interrupt vector init done. Going to read I/O port of 8042 for turbo switch (if any).
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data init is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is complete. Going for mono mode setting.
29	Monochrome mode setting is done. Going for Colour mode setting.
2A	Colour mode setting done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for setup before optional video ROM.
2C	Processing before video ROM control is done. Look for optional video ROM and give control.
2D	Optional video ROM control done. Give control to do processing after video ROM returns control.
2E	Return from processing after video ROM control. If EGA/VGA not found do display mem R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display mem R/W test passed. About to look for retrace checking.
31	Display mem R/W test/ retrace check failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. Looking for alternate display retrace checking.
33	Video display check over. Verification of display with switches and card to begin.
34	Verification of display adapter done. Display mode to be set next.
35	Display mode set complete. BIOS ROM data area about to be checked.
36	BIOS ROM data area check over. Going to set cursor for power on message.
37	Cursor setting for power on message id complete. Going to display power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the reference string.
3A	Reference string display is over. Going to display the Hit <Esc> message.
3B	Hit <Esc> message displayed. Virtual mode memory test about to start.
40	Preparation for virtual mode test started. Going to verify from video memory.
41	Returned after verifying from display memory. Going to prepare descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in the virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diag switch is on). Initialize data to check memory wrap around at 0:0.
45	Data initialized. Check for memory wrap around at 0:0and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. Writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k.
48	Patterns written in base memory. Going to find out amount of memory below 1Mb.
49	Amount of memory below 1Mb found and verified. Find out amount of memory above 1M memory.
4A	Amount of memory above 1Mb found and verified. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <Esc> and clear mem below 1Mb for soft reset.
4C	Memory below 1M cleared. (SOFT RESET). Going to clear memory above 1M.
4D	Memory above 1M cleared.(SOFT RESET). Going to save the memory size.
4E	Memory test started. (NO SOFT RESET). About to display first 64k memory test.
4F	Memory size display started, for update during memory test. Sequential and random memory test.
50	Memory test below 1Mb complete. Going to adjust memory size for relocation/ shadow.
51	Memory size adjusted due to relocation/shadow. Memory test above 1Mb to follow.

Code	Meaning
52	Memory test above 1Mb complete. Going to prepare to go back to real mode.
53	CPU registers are saved including memory size. Going to enter in real mode.
54	Shutdown successful. CPU in real mode. Restore registers saved during preparation for shutdown.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area about to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
58	BIOS ROM data area check over. Going to clear Hit <Esc>message.
59	Hit <Esc> message cleared. WAIT. . . message displayed.Sstart DMA and interrupt controller test.
60	DMA page register test passed. About to verify from display memory.
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clear output buffer, check for stuck key. About to issue keyboard reset
81	Keyboard reset error/stuck key found. About to issue keyboard controller i/f test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error; check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to CMOS setup program.
88	Returned from CMOS setup and screen cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8A	First screen message displayed. About to display WAIT. . . message.
8B	WAIT. . . message displayed. About to do Main and Video BIOS shadow.
8C	Main/Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed, mouse check and init to be done next
8E	Mouse check and initialisation complete. Going for hard disk floppy reset.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Memory size adjusted due to mouse support hdisk type 47. Going to verify from display memory.
96	Returned after verifying from display memory. Do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control next.
98	Optional ROM control done. Give control to do required processing after ROM returns control.
99	Iinitialization after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Copro test.
9C	Required initialization before coprocessor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after co-pro test complete. Going to check extd keyboard; ID and num-lock.
9F	Extd keyboard check done ID flag set. num-lock on/off. Keyboard ID command to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.

Code	Meaning
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Iinitialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display system configuration.
00	System configuration is displayed. Going to give control to INT 19h boot loader.

AMI New BIOS; 06/06/92-08/08/93

Code	Meaning
01	Processor register test about to start and NMI to be disabled.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete. Any initialization before keyboard BAT is in progress next.
04	Any init before keyboard BAT is complete. Reading keyboard SYS bit, to check soft reset/power on.
05	Soft reset/ power-on determined. Going to enable ROM; i.e. disable shadow RAM/Cache if any.
06	ROM enabled. Calculate ROM BIOS checksum - wait for 8042 keyboard controller input buffer to be free.
07	ROM BIOS checksum passed; KB controller input buffer free. Issue BAT command to keyboard controller.
08	BAT command to keyboard controller is issued. Going to verify the BAT command.
09	Keyboard controller BAT result verified. Keyboard command byte to be written next.
0A	Keyboard command byte code is issued. Going to write command byte data.
0B	Keyboard controller command byte written. Going to issue Pin 23/24 block/unblock command.
0C	Pin-23 & 24 of keyboard controller blocked/ unblocked. NOP command of controller to be issued next.
0D	NOP command processing is done. CMOS shutdown register test to be done next.
0E	CMOS shutdown register R/W test passed. Calculating CMOS checksum and update DIAG byte.
0F	CMOS checksum calc done; DIAG byte written. CMOS init begins (If INIT CMOS IN EVERY BOOT is set).
10	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
11	CMOS Status register initialised. Going to disable DMA and Interrupt controllers.
12	DMA controller #1 & #2, interrupt controller #1 & #2 disabled. Disable Video display and init port-B.
13	Disable Video display and initialise port B. Chipset init/auto memory detection about to begin.
14	Chipset initialization/auto memory detection over. 8254 timer test about to start.
15	CH-2 timer test halfway. 8254 CH-2 timer test to be complete.
16	Ch-2 timer test over. 8254 CH-1 timer test to be complete.
17	CH-1 timer test over. 8254 CH-0 timer test to be complete.
18	CH-0 timer test over. About to start memory refresh.
19	Memory Refresh started. Memory Refresh test to be done next.
1A	Memory Refresh line is toggling. Going to check 15 microsecond ON/OFF time.
1B	Memory Refresh period 30 microsecond test complete. Base 64K memory test about to start.
20	Base 64k memory test started. Address line test to be done next.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test.
23	Base 64k sequential data R/W test passed. Any setup before Interrupt vector init about to start.
24	Setup required before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read I/O port of 8042 for turbo switch (if any).

Code	Meaning
26	I/O port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data initialization is over. Any initialization after interrupt vector to be done next.
28	Initialization after interrupt vector is complete. Going for monochrome mode setting.
29	Monochrome mode setting is done. Going for Colour mode setting.
2A	Colour mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for any setup required before optional video ROM check.
2C	Processing before video ROM control done. Looking for optional video ROM and give control.
2D	Optional video ROM control done. Giving control for processing after video ROM returns control.
2E	Return from processing after video ROM control. If EGA/VGA not found test display mem R/W.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display mem R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. Looking for the alternate display retrace checking.
33	Video checking over. Verification of display type with switch setting and actual card to begin.
34	Verification of display adapter done. Display mode to be set next.
35	Display mode set complete. BIOS ROM data area about to be checked.
36	BIOS ROM data area check over. Going to set cursor for power on message.
37	Cursor setting for power on message complete. Going to display power on message.
38	Power on message display complete. Going to read new cursor position.
39	New cursor position read and saved. Going to display the reference string.
3A	Reference string display over. Going to display the Hit <ESC> message.
3B	Hit <ESC> message displayed. Virtual mode memory test about to start.
40	Preparation for virtual mode test started. Going to verify from video memory.
41	Returned after verifying from display memory. Going to prepare descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diags switch on). Going to initialize data to check mem wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding total memory size.
46	Mem wrap around test done. Size calculation over. Going for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M.
49	Amount of memory below 1Mb found and verified. Going to find amount of memory above 1Mb.
4A	Amount of memory above 1Mb found and verified. Going for BIOS ROM data area check.
4B	BIOS ROM data area check over. Going to check <Esc>, clear mem below 1 Mb for soft reset.
4C	Memory below 1Mb cleared. (SOFT RESET). Going to clear memory above 1 Mb.
4D	Memory above 1Mb cleared. (SOFT RESET). Going to save memory size.
4E	Memory test started. (NO SOFT RESET). About to display first 64K memory test.
4F	Memory size display started, updated during memory test. Going for sequential and random memory test.
50	Memory test below 1Mb complete. Going to adjust memory size for relocation/shadow.
51	Memory size adjusted due to relocation/shadow. Memory test above 1Mb to follow.
52	Memory test above 1Mb complete. Preparing to go back to real mode.
53	CPU registers saved including memory size. Going to enter real mode.
54	Shutdown successful; CPU in real mode. Restore registers saved during shutdown prep.
55	Registers restored. Going to disable gate A20 address line.
56	A20 address line disable successful. BIOS ROM data area about to be checked.
57	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
58	BIOS ROM data area check over. Going to clear Hit <ESC> message.
59	Hit <ESC> message cleared. <WAIT...> message displayed. About to start DMA and PIC test.
60	DMA page register test passed. About to verify from display memory.

Code	Meaning
61	Display memory verification over. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
63	DMA #2 base register test passed. About to go for BIOS ROM data area check.
64	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
65	BIOS ROM data area check over. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
80	Keyboard test started. Clearing output buffer, checking for stuck key. Issue keyboard reset.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written, Global data init done. About to check for lock-key.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Going to CMOS setup program.
88	Returned from CMOS setup program, screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8A	First screen message displayed. About to display <WAIT...> message.
8B	<WAIT...> message displayed. About to do Main and Video BIOS shadow.
8C	Main/Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options programmed; mouse check and initialisation to be done next.
8E	Mouse check and initialisation complete. Going for hard disk and floppy reset.
8F	Floppy check returns that floppy is to be initialized. Floppy setup to follow.
90	Floppy setup is over. Test for hard disk presence to be done.
91	Hard disk presence test over. Hard disk setup to follow.
92	Hard disk setup complete. About to go for BIOS ROM data area check.
93	BIOS ROM data area check halfway. BIOS ROM data area check to be complete.
94	BIOS ROM data area check over. Going to set base and extended memory size.
95	Mem size adjusted due to mouse support, hard disk type 47. Going to verify from display memory.
96	Returned after verifying display memory. Doing any init before C800 optional ROM control
97	Any init before C800 option ROM control over. ROM check and control will be done next.
98	Optional ROM control done. Give control for required processing after ROM returns control.
99	Init required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before co-processor over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Initialization after copro test complete. Check extd keyboard, keyboard ID and num lock.
9F	Extd keyboard check is done, ID flag set. num lock on/off. Keyboard ID command to be issued.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Screen to be cleared next.
A6	Screen cleared. Going to enable parity and NMI.
A7	NMI and parity enabled. Going to do any init before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Do any initialisation after E000 optional ROM control.

Code	Meaning
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
00	System configuration is displayed. Going to give control to INT 19h boot loader.

AMI WinBIOS; 12/15/93 Onwards

Code	Meaning
01	Processor register test about to start; disable NMI next.
02	NMI is Disabled. Power on delay starting.
03	Power on delay complete (to check soft reset/power-on).
05	Soft reset/power-on determined, enable ROM (i.e. disable shadow RAM cache, if any).
06	ROM is enabled. Calculating ROM BIOS checksum.
07	ROM BIOS checksum passed. CMOS shutdown register test to be done next.
08	CMOS shutdown register test done. CMOS checksum calculation next.
09	CMOS checksum calculation done; CMOS diag byte written; CMOS initialisation to begin.
0A	CMOS initialization done (if any). CMOS status register about to init for Date and Time.
0B	CMOS status register init done. Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. Going to issue the BAT command to keyboard controller.
0D	BAT command to keyboard controller is issued. Going to verify the BAT command.
0E	Keyboard controller BAT result verified. Any initialization after KB controller BAT next.
0F	Initialisation after KB controller BAT done. Keyboard command byte to be written next.
10	Keyboard controller command byte written. Going to issue Pin 23 & 24 block/unblock command.
11	Keyboard controller Pin 23/24 blocked/unblocked; check press of <INS> key during power-on .
12	Checking for pressing of <Ins> key during power-on done. Disabling DMA/Interrupt controllers.
13	DMA controller #1 and #2 and Interrupt controller #1 and #2 disabled; video display disabled and port B initialised; chipset init/auto memory detection next.
14	Chipset init/auto memory detection over. To uncompress the POST code if compressed BIOS.
15	POST code is uncompressed. 8254 timer test about to start.
19	8254 timer test over. About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time.
20	Memory Refresh 30 microsecond test complete. Base 64K memory/address line test about to start.
21	Address line test passed. Going to do toggle parity.
22	Toggle parity over. Going for sequential data R/W test on base 64k memory.
23	Base 64k sequential data R/W test passed. Setting BIOS stack and any setup before Interrupt
24	Setup required before vector initialization complete. Interrupt vector initialization about to begin.
25	Interrupt vector initialization done. Going to read Input port of 9042 for turbo switch and clear password if POST diag switch is ON next.
26	Input port of 8042 is read. Going to initialize global data for turbo switch.
27	Global data init for turbo switch over. Any initialization before setting video mode next.
28	Initialization before setting video mode complete. Going for mono mode and colour mode setting.
2A	Mono and colour mode setting is done. About to go for toggle parity before optional ROM test.
2B	Toggle parity over. About to give control for setup before optional video ROM check next.
2C	Processing before video ROM control done. About to look for video ROM and give control.
2D	Video ROM control done. About to give control for processing after video ROM returns control.
2E	Return from processing after video ROM control. If EGA/VGA not found do display mem R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display mem R/W test or retrace checking failed. About to do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. Looking for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.

Code	Meaning
37	Display mode set. Going to display the power on message.
39	New cursor position read and saved. Going to display the Hit <DEL> message.
3B	Hit <DEL> message displayed. Virtual mode memory test about to start.
40	Going to prepare the descriptor tables.
42	Descriptor tables prepared. Going to enter in virtual mode for memory test.
43	Entered in virtual mode. Going to enable interrupts for diagnostics mode.
44	Interrupts enabled (if diags switch on). Going to initialize data to check mem wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and find total system memory.
46	Memory wrap around test done. Memory size calculation over. Go for patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find amount of memory below 1Mb.
49	Amount of memory below 1Mb found and verified. Finding amount of memory above 1Mb memory.
4B	Memory above 1Mb verified. Check for soft reset and going to clear memory below 1Mb for soft reset next (if power on go to POST # 4Eh).
4C	Memory below 1Mb cleared.(SOFT RESET)
4D	Memory above 1Mb cleared.(SOFT RESET); save memory size next (go to POST # 52h).
4E	Memory test started. (NOT SOFT RESET); display first 64K memory size next.
4F	Memory size display started.Will be updated during memory test; sequential and random memory test next.
50	Memory testing/initialisation below 1Mb complete. Adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1Mb to follow.
52	Memory testing/initialisation above 1Mb complete. Going to save size information.
53	Memory size is saved. CPU registers are saved. Going to enter real mode.
54	Shutdown successful, CPU in real mode, disable gate A20 line next.
57	A20 address line disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. Start DMA and interrupt controller test.
60	DMA page register test passed. About to go for DMA #1 base register test.
62	DMA #1 base register test passed. About to go for DMA #2 base register test.
65	DMA #2 base register test passed. About to program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. About to initialize 8259 interrupt controller.
67	8259 initialization over. About to start keyboard test.
F4	Extended NMI sources enabling is in progress (EISA).
80	Keyboard test. Clear output buffer; check for stuck key; issue reset keyboard command next.
81	Keyboard reset error/stuck key found. About to issue keyboard controller interface test command.
82	Keyboard controller interface test over. About to write command byte and init circular buffer.
83	Command byte written; global data init done; check for lock-key next.
84	Lock-key checking over. About to check for memory size mismatch with CMOS.
85	Memory size check done. About to display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. Uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power on screen message.
8B	First screen msg displayed. <Wait...> message displayed. About to do Main/Video BIOS shadow.
8C	Main/Video BIOS shadow successful. Setup options programming after CMOS setup about to start.
8D	Setup options are programmed; mouse check and init next.
8E	Mouse check and initialisation complete. Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
94	Hard disk setup complete. Going to set base and extended memory size.

Code	Meaning
96	Memory size adjusted for mouse support, hard disk type 47; init before C800, optional ROM next.
97	Init before C800 ROM control is over. Optional ROM check and control next.
98	Optional ROM control done. Give control for required processing after optional ROM returns control next.
99	Iinitialization required after optional ROM test over. Setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test.
9C	Required initialization before co-processor is over. Going to initialize the coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after coprocessor test.
9E	Init after coprocessor test complete. Going to check extd keyboard; keyboard ID and NumLock.
9F	Extd keyboard check is done; ID flag set; NumLock on/off, issue keyboard ID command next.
A0	Keyboard ID command issued. Keyboard ID flag to be reset.
A1	Keyboard ID flag reset. Cache memory test to follow.
A2	Cache memory test over. Going to display any soft errors.
A3	Soft error display complete. Going to set the keyboard typematic rate.
A4	Keyboard typematic rate set. Going to program memory wait states.
A5	Memory wait states programming over. Going to clear the screen and enable parity/NMI.
A7	NMI and parity enabled.Ddo any initialization required before giving control to optional ROM at E000 next.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do init required.
AA	Init after E000 optional ROM control is over. Going to display the system configuration.
B0	System configuration is displayed. Going to uncompress SETUP code for hot-key setup.
B1	Uncompressing of SETUP code is complete. Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT 19h boot loader.

EISA

Code	Meaning
F0	Initialisation of I/O cards in slots is in progress (EISA).
F1	Extended NMI sources enabling is in progress (EISA).
F2	Extended NMI test is in progress (EISA).
F3	Display any slot initialisation messages.
F4	Extended NMI sources enabling in progress.

10/10/94

Code	Meaning
C2	NMI is Disabled. Power on delay starting
C5	Power on delay complete. Going to disable Cache if any
C6	Calculating ROM BIOS checksum
C8	CMOS shutdown register test done. CMOS checksum calculation to be done next
CA	CMOS checksum calc done, CMOS Diag byte written. CMOS status register to init for Date and Time
CB	CMOS status register init done. Any initialization before keyboard BAT to be done next
CD	BAT command to keyboard controller is to be issued
CE	Keyboard controller BAT result verified. Any initialization after KB controller BAT to be done next
CF	Initialization after KB controller BAT done. Keyboard command byte to be written next
D1	Keyboard controller command byte is written. Going to check pressing of INS key during power-on
D2	Checking for pressing of INS key during power-on done. Disabling DMA and Interrupt controllers
D3	DMA controller #1,#2, interrupt controller #1,#2 disabled. Chipset init auto memory detection now

Code	Meaning
D4	Chipset initialization/auto memory detection over. To uncompress the RUNTIME code
D5	RUNTIME code is uncompressed
DD	Transfer control to uncompressed code in shadow ram at F000:FFF0h

RUNTIME CODE IS UNCOMPRESSED IN F000H SHADOW RAM

Code	Meaning
03	NMI is Disabled. To check soft reset/power-on
05	Soft reset/power-on determined. Going to disable Cache if any
06	POST code to be uncompressed
07	POST code is uncompressed. CPU init and CPU data area init to be done next
08	CPU and CPU data area init done. CMOS checksum calculation to be done next
09	CMOS checksum done, Diag byte written. CMOS init begin (If "Init CMOS in every boot" set)
0A	CMOS initialization done (if any). CMOS status register about to init for Date and Time
0B	CMOS status register init done. Any initialization before keyboard BAT to be done next
0C	KB controller I/B free. Going to issue the BAT command to keyboard controller
0D	BAT command to keyboard controller is issued. Going to verify the BAT command
0E	Keyboard controller BAT result verified. Initialization after KB controller BAT to be done next
0F	Initialization after KB controller BAT done. Keyboard command byte to be written next
10	Keyboard controller command byte is written. Issue Pin-23,24 blocking/unblocking command
11	Pin-23,24 of keyboard controller blocked/ unblocked. Check pressing of INS key on power-on
12	Check for pressing of INS key during power-on done. Disable DMA and Interrupt controllers
13	DMA controller #1,#2, interrupt controller #1,#2 disabled. Video display is disabled and port-B is initialized.Chipset init about to begin
15	Chipset initialization over. 8254 timer test to start. 8254 timer test over. Start refresh test
1A	Memory Refresh line is toggling. Going to check 15 micro second ON/OFF time
20	Memory Refresh period 30 micro second test complete. Base 64K memory to be initialized
23	Base 64K memory initialized. SDet BIOS stack and to do any setup before Interrupt vector init
24	Setup required before interrupt vector init complete. Interrupt vector initialization to begin
25	Interrupt vector initialization done. Going to read Input port of 9042 for turbo switch (if any) and to clear password if post diag switch is on
26	Input port of 8042 is read. Going to initialize global data for turbo switch
27	Global data initialization for turbo switch over. Initialization before setting video mode next
28	Initialization before setting video mode complete. Monochrome mode and color mode setting
2A	Different Buses init (system, static, output devices) to start if present
2B	About to give control for any setup required before optional video ROM check
2C	Processing before video ROM control is done. Look for optional video ROM and give control
2D	Optional video ROM control done. Give control for processing after video ROM returns control
2E	Back after video ROM control. If EGA/VGA not found do display mem R/W test
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memory R/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed.Ddo alternate Display memory R/W test
32	Alternate Display memory R/W test passed. Look for the alternate display retrace checking
34	Video display checking over. Display mode to be set next
37	Display mode set. Going to display the power on message
38	Different Buses init (input, IPL, general devices) to start if present.
39	Display different Buses initialization error messages.
3A	New cursor position read and saved. Going to display the Hit DEL message
3B	Hit DEL message displayed. Virtual mode memory test about to start

Code	Meaning
40	Going to prepare the descriptor tables
42	Descriptor tables prepared. Going to enter in virtual mode for memory test
43	Entered protected mode. Enabling interrupts for diagnostics mode next
44	Interrupts enabled if diag switch is on. Initializing to check memory wraparound at 0:0 next
45	Data initialized. Check for memory wraparound at 0:0 and find the total system memory size
46	Memory wraparound test done. Size calculation done. Writing patterns to test memory
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory
48	Patterns written in base memory. Going to findout amount of memory below 1M memory
49	Memory below 1Mb found and verified.Find out amount of memory above 1M memory
4B	Amount of memory above 1Mb found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point# 4Eh)
4C	Memory below 1Mb cleared. (SOFT RESET) Going to clear memory above 1M
4D	Memory above 1Mb cleared. (SOFT RESET) Save the memory size. (Go to check point# 52h)
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size
50	Memory testing/initialization below 1Mb complete. Adjust memory size for relocation/ shadow
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow
52	Memory testing/initialization above 1Mb complete. Going to save memory size information
53	The memory size information and the CPU registers are saved. Entering real mode next
54	Shutdown successful, CPU in real mode. Disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Adjust memory size on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear Hit DEL message
59	Hit DEL message cleared. WAIT... message displayed. Start DMA and interrupt controller test
60	DMA page register test passed. To do DMA#1 base register test
62	DMA#1 base register test passed. To do DMA#2 base register test
65	DMA#2 base register test passed. To program DMA unit 1 and 2
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller
67	8259 initialization over
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. clearing output buffer, checking for stuck key. Issue keyboard reset
81	Keyboard reset error/stuck key. About to issue keyboard controller interface test command
82	Keyboard controller interface test over. About to write command byte and init circular buffer
83	Command byte written. Global data init done. About to check for lock-key
84	Lock-key checking over. About to check for memory size mismatch with CMOS
85	Memory size check done. About to display soft error and check for password or bypass setup
86	Password checked. About to do programming before setup
87	Programming before setup complete. Uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power on screen message
8B	First screen message displayed WAIT message displayed. About to do Video BIOS shadow
8C	Video BIOS shadow successful. Setup options programming after CMOS setup about to start
8D	Setup options are programmed, mouse check and init to be done next
8E	Mouse check and initialization complete. Going for hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup to be done next
94	Hard disk setup complete. To set base and extended memory size
95	Memory size adjusted for mouse support. Init of different buses optional ROMs from C800
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control next
98	Optional ROM control done. Give control for processing after optional ROM returns control

Code	Meaning
99	Any init required after optional ROM test over. Setup timer data area and printer base address
9A	Return after setting timer and printer base address. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test
9E	Initialization after coprocessor test complete. Check extd keyboard, keyboard ID and num-lock
9F	Extd keyboard check is done, ID flag set, num-lock on/off. Keyboard ID command to be issued
A0	Keyboard ID command issued. ID flag to be reset. A1 Keyboard ID flag reset. Cache test next
A2	Cache memory test over. Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Memory wait states programming over. Going to clear the screen and enable parity/NMI
A7	NMI and parity enabled. Do initialization required before giving control to ROM at E000h
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Initialization required after E000 optional ROM control
AA	Initialization after E000 ROM control is over. Going to display the system configuration
B0	System configuration is displayed
B1	Going to copy any code to specific area
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next

Version 6.2 - 7/15/95

Valid for all AMI products with a core BIOS date of 7/15/95. Control is passed to different buses at 2A, 38, 39 and 95, where additional checkpoints are output to port 80 as word to identify the routines being executed. These are word checkpoints - the low byte is where control is passed, and the high byte contains this information:

Bits	Meaning
7-4	0000 Function 0. Disable all devices on the bus 0001 Function 1. Init static devices 0010 Function 2. Init output devices 0011 Function 3. Init input devices 0100 Function 4. Init IPL devices 0101 Function 5. Init general devices 0110 Function 6. Init error reporting 0111 Function 7. Init add-on ROMs
3-0	Specify the bus: 0 Generic DIM device Init Manager 1 Onboard system devices 2 ISA devices 3 EISA devices 4 ISA PnP devices 5 PCI devices

UNCOMPRESSED INITIALISATION CODES

Code	Meaning
D0h	NMI is disabled, power on delay starting. Init code checksum to be verified next
D1h	Init DMA controller,do keyboard controller BAT test, start memory refresh, 4 Gb flat mode next
D3h	Start memory sizing next
D4h	Return to real mode. Execute OEM patches and set stack.

Code	Meaning
D5h	Passing control to uncompressed code in Shadow RAM at E000:0000h. Init code is copied to segment 0 and control will be transferred to it.
D6h	Control is in segment 0.Next, checking if Ctrl-Home was pressed and verifying BIOS checksum. If keys were pressed or checksum is bad, next will go to checkpoint code E0h. Otherwise, go to D7h
DD	Early initialization super IO chips that contain disabled at power on RTC and KBC
D0	NMI disabled. Power on delay starting. Next, the initialization code checksum will be verified
D1	Initializing the DMA controller, performing the keyboard controller BAT test, starting memory refresh, and entering 4 GB flat mode next
D3	Starting memory sizing next
D4	Returning to real mode. Executing any OEM patches and setting the stack next
D5	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0
D6	Control is in segment 0. Next, checking if CTRL HOME was pressed and verifying the system BIOS checksum. If either CTRL HOME was pressed or the system BIOS checksum is bad, next will go to checkpoint code E0h. Otherwise, going to checkpoint code D7h.
D7	Passing control to the interface module next
D8	The main system BIOS runtime code will be decompressed next
D9	Passing control to the main system BIOS in shadow RAM next

BOOTBLOCK RECOVERY CODES

Code	Meaning
E0h	FD controller initialized. Next, beginning base 512K memory test.
E1h	Init interrupt vector table next
E2h	Init DMA and interrupt controllers next
E6h	Enabling FD controller and timer IRQs. Enabling internal cache memory
EDh	Init floppy drive
EEh	Looking for floppy in drive A:. Reading first sector
EFh	Read error from floppy in A:
F0h	Next, searching for AMIBOOT ROM file in root directory
F1h	AMIBOOT ROM file not in root directory
F2h	Next, reading and analyzing floppy FAT to find clusters occupied by AMIBOOT ROM file
F3h	Next, reading AMIBOOT ROM file, cluster by cluster
F4h	AMIBOOT ROM file not the correct size
F5h	Next, disabling internal cache
FBh	Next, detecting type of flash ROM
FCh	Next, erasing flash ROM
FDh	Next, programming flash ROM
FFh	Flash ROM programming successful. Next, restarting System BIOS

UNCOMPRESSED INITIALISATION CODES IN F0000H SHADOW RAM

Code	Meaning
03	NMI disabled. Next, checking for soft reset or power on
05	BIOS stack has been built. Next, disabling cache
06	Uncompressing POST code
07	Init CPU and CPU data area
08	CMOS checksum calculation next

Code	Meaning
0A	CMOS checksum calculation done. Init CMOS status register for data and time next
0B	CMOS status register initialized. Next, performing init before keyboard BAT command issued
0C	Keyboard controller input buffer is free. Next, issuing BAT command to keyboard controller
0E	Keyboard controller BAT command verified. Next, performing any necessary init after BAT test
0F	init after BAT test done. Keyboard command byte written next
10	Keyboard controller command byte written. Next, pin 23/ 24 blocking/unblocking command
11	Next, checking if End or Ins keys were pressed during power on. Init CMOS RAM if if Initialise CMOS RAM in every boot POST option was set in AMIBCP or End key was pressed.
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2
13	Video display disabled and port B initialized. Next, init chipset.
14	8254 timer test next
19	8254 timer test over. Starting memory refresh test.
1A	Memory refresh line toggling. Checking 15 second on/off time.
23	Reading 8042 input port and disabling MEGAKEY Green PC feature next. Making BIOS Code segment writable and performing necessary configuration before initializing interrupt vectors.
24	Configuration required before interrupt vector init completed. Interrupt vector init begins.
25	Interrupt vector init done. Clearing password if the POST DIAG switch is on.
27	Any init before setting video mode will be done next.
28	Init before setting video mode is complete.
2A	Bus init system, static, output devices will be done next, if present.
2B	Passing control to video ROM to perform any required configuration before video ROM test.
2C	All necessary processing before passing control to Video ROM is done. Looking for Video ROM next and passing control to it.
2D	Video ROM returned control to POST.Doing required processing after Video ROM had control.
2E	Completed post-video ROM test processing. If EGA/VGA controller is not found, performing display memory read/write test next.
2F	EGA/VGA controller was not found. Display memory read/write test is about to begin.
30	Display memory read/write test passed. Look for retrace checking next.
31	Display memory read/write test or retrace checking failed. Performing alternate display memory read/write test.
32	Alternate display memory read/write test passed. Look for alternat display retrace check next.
34	Video display checking over. Setting display mode next.
37	Display mode set. Displaying power on message next.
38	Initialising bus input, IPL, general devices next, if present.
39	Displaying bus init error messages.
3A	New cursor position read and saved. Displaying the Hit <Del> message next.
3B	Hit <Del> message displayed. Protected mode memory test about to start.
40	Preparing descriptor tables next.
42	Descriptor tables prepared. Entering protected mode for memory test next.
43	Entered protected mode. Enabling interrupts for diags mode next.
44	Interrupts enabled if diags switch is on. Initialising data to check memory wraparound at 0:0
45	Data initialized. Check for memory wraparound at 0:0 and find total system memory size next.
46	Memory wraparound test done. Mem size calculation done. Writing patterns to test memory
47	Memory pattern has been written to extended memory. Writing patterns to base 640K next.
48	Patterns written in base memory. Determining memory below 1 Mb next.
49	Memory below 1 Mb found and verified. Determining memory above 1 Mb next.
4B	Memory above 1 Mb verified. Checking for soft reset, clearing memory below 1 Mb for soft reset next. If power on, checking 4Eh next.
4C	Memory below 1 Mb cleared via soft reset. Clearing memory above 1 Mb next.
4D	Memory above 1 Mb cleared via soft reset. Saving memory size next. 52h next.

Code	Meaning
4E	Memory test started, but not as result of soft reset. Displaying first 64K memory size next.
4F	Memory size display started. Display updated during test.Performing sequential and random memory test next.
50	Memory below 1 Mb tested and initialized. Adjusting displayed memory size for relocation and shadowing next.
51	Memory size display adjusted for relocation and shadowing. Testing memory above 1 Mb.
52	Memory above 1 Mb tested and initialized. Saving memory size information next.
53	Memory size information and CPU registers are saved. Entering real mode next.
54	Shutdown successful, CPU in real mode. Disabling Gate A20 line, parity and NMI next.
57	Gate A20 line, parity and NMI disabled. Adjust memory size on relocation and shadowing next.
58	Adjusted memory size depending on relocation and shadowing. Clearing Hit <Del> message.
59	Hit <Del> message cleared. <Wait> message displayed.
60	DMA page register test passed.
62	DMA controller 1 base register test passed.
65	DMA controller 2 base register test passed.
66	Completed programming DMA controllers 1 and 2.
67	Completed 8259 interrupt controller init.
7F	Extended NMI source enabling in progress
80	Keyboard test started. Clearing output buffer and checking for stuck keys.
81	Keyboard reset error or stuck key found.
82	Keyboard controller interface test completed.
83	Command byte written and global data init completed
84	Locked key checking over.
85	Memory size check done.
86	Password checked.
87	Programming before WINBIOS setup complete.
88	Returned from WINBIOS setup and cleared screen.
89	Programming after WINBIOS setup completed.
8B	First screen power on message displayed, and <Wait> message. PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming WINBIOS setup options next.
8D	WINBIOS setup options programmed.
8F	HD controller reset.
91	FD controller configured.
95	Initialising bus option ROMs from C800 next.
96	Init before passing control to adapter ROM at C800
97	Init before C800 ROM gains control completed.
98	Adapter ROM has passed control back to BIOS POST. Performing required programming.
99	Init required after ROM test now complete.
9A	Set timer and printer base addresses.
9B	RS232 base address set.
9C	Required init before coprocessor test over.
9D	Coprocessor initialized.
9E	Init after copro test complete. Checking extended keyboard, keyboard ID and Num Lock key next. Issuing keyboard ID command next.
A2	Displaying soft errors next.
A3	Soft error display complete.
A4	Keyboard typematic rate set.
A5	Memory wait state programming over.

Code	Meaning
A7	Screen cleared, NMI and parity enabled.Init before passing control to ROM at E000 complete. Passing control to E000 next.
A8	Init before E000 control complete.
A9	Returned from E000 control.
AA	Init after E000 control complete. Displaying system configuration next.
AB	Uncompressing DMI data and executing DMI POST init next.
B0	System configuration displayed
B1	Copying code to specific areas.
00	Code copying done. Passing control to INT 19 boot loader next.

ARCHE TECHNOLOGIES

Legacy BIOS

Derives from AMI (9 April 90), using port 80; certain codes come up if a copy is made without AMI's copyright notice. The major differences are at the end.

Code	Explanation
01	Disable NMI and test CPU registers
02	Verify ROM BIOS checksum (32K at F800:0)
03	Initial keyboard controller and CMOS RAM communication
04	Disable DMA and interrupt controllers; test CMOS RAM interrupt
05	Reset Video
06	Test 8254 timer
07	Test delta count for timer channel 2 (speaker)
08	Test delta count for timer channel 1 (memory refresh)
09	Test delta count for timer channel 0 (system timer)
0A	Test parity circuit and turn on refresh
0B	Enable parity check circuit and test system timer
0C	Test refresh trace link toggle
0D	Test refresh timing synchronization of high and low period
10	Disable cache and shadow BIOS; test 64K base memory address lines
11	Test base 64K memory for random addresses and data read/write
12	Initialize interrupt vectors in lower 1K of RAM
14	Test CMOS RAM shutdown register read/write; disable DMA and interrupt controllers
15	Test CMOS RAM battery and checksum, and different options such as diagnostic byte
16	Test floppy information in CMOS RAM; initialize monochrome video
17	Initialise colour video
18	Clear parity status if any
19	Test for EGA/VGA video ROM BIOS at C000:0 and pass control to it if there
1A	Returned from video ROM. Clear parity status if any; update system parameters for any video ROM found; test display memory read/write
1B	Primary video adapter: check vertical/horizontal retrace; write/read test video memory
1C	Secondary video adapter: check vertical and horizontal retrace; write/read test video memory
1D	Compare and verify CMOS RAM video type with switches and video adapter; set equipment byte if correct
1E	Call BIOS to set mono/colour video mode according to CMOS RAM

Code	Explanation
20	Display CMOS RAM write/read errors and halt if any
21	Set cursor to next line and call INT 10 to display
22	Display Power on 386 BIOS message and check CPU speed is 25 or 33 MHz
23	Read new cursor position and call INT 10 to display
24	Skip 2 rows of text and display (C)AMI at bottom of screen
25	Refresh is off, so call shadow RAM test
F0	Failure inside shadow RAM test
30	Verify (C)AMI... and overwrite with blanks before entering protected mode
31	Enter protected mode and enable timer interrupt (IRQ0). Errors indicate gate A20 circuit failed
32	Size memory above 1Mb
33	Size memory below 640K
34	Test memory above 1Mb
35	Test memory below 1Mb
36	Unknown AMI function
37	Clear memory below 1Mb
38	Clear memory above 1Mb
39	Set CMOS shutdown byte to 3 and go back to real mode
3A	Test sequential and random data write/read of base 64K RAM
3B	Test RAM below 1Mb and display area being tested
3C	Test RAM above 1Mb and display area being tested
3D	RAM test OK
3E	Shutdown for return to real mode
3F	Back in real mode; restore all variables
40	Disable gate A20 since now in real mode
41	Check for (C)AMI in ROM
42	Display (C)AMI message
43	Clear <Esc> message; test cache
4E	Process shutdown 1; go back to real mode
4F	Restore interrupt vectors and global data in BIOS RAM area
50	Test 8237 DMA controller and verify (c)AMI in ROM
51	Initialize DMA controller
52	Test various patterns to DMA controller
53	Verify (C)AMI in ROM
54	Test DMA control flip-flop
55	Initialize and enable DMA controllers 1 and 2
56	Initialize 8259 interrupt controllers-clear write request and mask registers
57	Test 8259 controllers and setup interrupt mask registers
61	Check DDNIL status bit and display message if clear
70	Perform keyboard BAT (Basic Assurance Test)
71	Program keyboard to AT type
72	Disable keyboard and initialize keyboard circular buffer
73	Display DEL message for setup prompt and initialize floppy controller/drive
74	Attempt to access floppy drive
75	If CMOS RAM is good, check and initialize hard disk type identified in CMOS RAM
76	Attempt to access hard disk and set up hard disk
77	Shuffle any internal error codes
78	Verify (C)AMI is in ROM
79	Check CMOS RAM battery and checksum; clear parity status
7A	Compare size of base/extended memory to CMOS RAM info

Code	Explanation
7B	Unknown AMI function
7C	Display (C)AMI
7D	Set/reset AT compatible memory expansion bit
7E	Verify (C)AMI is in ROM
7F	Clear <DEL> message from screen and check if DEL pressed
80	Find option ROM in C800 to DE00 and pass control to any found
81	Return from adapter ROM; initialize timer and data area
82	Setup parallel and serial port base info in global data area
83	Test for presence of 80387 numeric coprocessor and initialize
84	Check lock key for keyboard
85	Display soft error messages if CMOS RAM data error was detected (battery or checksum)
86	Test for option ROM in E000:0 and pass control to any found
A0	Error in 256 Kbit or 1Mbit RAM chip in lower 640K memory
A1	Base 64K random address/data pattern test (only in 386APR and Presto 386SX)
A9	Initialize on-board VGA (Presto 386SX)
B0	Error in 256 Kbit RAM chip in lower 640K memory
B1	Base 64K random address/data pattern test (only in Presto 386SX BIOS)
E0	Returned to real mode; initialise base 64K RAM (Presto)
E1	initialize base 640K RAM (Presto)
EF	Configuration memory error in Presto -can't find memory
F0	Test shadow RAM from 0:4000 RAM area
00	Call INT 19 boot loader

AST

See also Phoenix or (mostly) Award. AST introduced an enhanced BIOS in 1992 with 3 beeps before all early POST failure messages, for Field Replaceable Unit identification. Otherwise, the most significant (left) digit of the POST code indicates the number of long beeps, and the least significant (right) digit indicates the short beeps. 17 therefore means 1 long beep and 7 short. Doesn't work after 20. Errors below 20 are generally fatal.

Early POST Codes

These are usually fatal and accompanied by a beep code:

Code	Meaning
1	System Board
2	SIMM Memory; System Board
3	SIMM Memory; System Board
4	SIMM Memory; System Board
5	Processor; System Board
6	Keyboard Controller; System Board
7	Processor; System Board
8	Video Adapter; Video RAM; System Board
9	BIOS; System Board
10	System Board
11	External cache; System Board

Code	Meaning
00	Reserved
	Beep and Halt if Error occurs
01	Test CPU registers and functionality
02	Test empty 8042 keyboard controller buffer
03	Test 8042 keyboard controller reset
04	Verify keyboard ID and low-level keyboard communication
05	Read keyboard input port (WS386SX16 only)
06	Initialise system board support chipset
09	Test BIOS ROM checksum; flush external cache
0D	Test 8254 timer registers (13 short beeps)
0E	Test ASIC registers (CLEM only, 14 short beeps)
0F	Test CMOS RAM shutdown byte (15 short beeps)
10	Test DMA controller 0 registers
11	Test DMA controller 1 registers
12	Test DMA page registers (see code 17)
13	see code 17
14	Test memory refresh toggle (see code I7)
15	Test base 64K memory
16	Set interrupt vectors in base memory
17	Init video; if EGA/VGA, issue code 12-13 if error, but only use this POST code beep pattern
12	EGA/VGA vertical retrace failed (different from normal beep)
13	EGA/VGA RAM test failed (different than normal beep tone)
14	EGA/VGA CRT registers failed (different than normal beep)
18	Test display memory
	Don't beep and don't halt if error occurs
20	EISA bus board power up (EISA Systems only)
30	Test interrupt controller #1 mask register
31	Test interrupt controller #2 mask register
32	Test interrupt controllers for stuck interrupt
33	Test for stuck NMI (P386 25/33, P486, CLEM and EISA)
34	Test for stuck DDNIL status bit (CLEM only)
40	Test CMOS RAM backup battery
41	Calculate and verify CMOS RAM checksum
42	Setup CMOS RAM options (except WS386SX16)
50	Test protected mode
51	Test protected mode exceptions
60	Calculate RAM size
61	Test RAM
62	Test shadow RAM (WS386SXI6, P386 25/33, P486, CLEM, EISA), or test cache (P386/I6)
63	Test cache (P38625/33, P486, CLEM, EISA), or copy system BIOS to shadow RAM (P386C, P386/I6, WS386SX16)
64	Copy system BIOS to shadow RAM (P386 25/33, P486, CLEM, EISA), or copy video BIOS to shadow RAM (P38616, SW386SX16)
65	Copy video BIOS to shadow RAM (P386 25/33, P486, CLEM, EISA), or test cache (WS386SX16)
66	Test 8254 timer channel 2 (P386 25/33, P486, EISA)
67	Initialize memory (Eagle only)

AT&T

Phoenix or Olivetti (M24 for early 6300s , and Phoenix for Intel boards). After 1991, NCR.

Code	Meaning	Code	Meaning
01	CPU Test	25	Unexpected Interrupt
02	System I/O Port	26	Expected Interrupt
03	ROM Checksum	30	Protected Mode for AT-Bus or Base Memory
05	DMA Page Register	31	Size of AT-Bus or External Memory
06	Timer 1	32	Address Lines A16..A23
07	Timer 2	33	Internal Memory or Conventional Memory Test
08	RAM Refresh	34	AT-Bus Memory Test or External Memory Test
09	8/19-Bit Bus Conversion	38	Shadow ROM BIOS
0A	Interrupt Controller 1	39	Shadow Extension BIOS
0B	Interrupt Controller 2	40	Enable/Disable Keyboard
0C	Keyboard Controller	41	Keyboard Clock and Data
0D	CMOS RAM/RTC	42	Keyboard Reset
0E	Battery Power Lost	43	Keyboard Controller
0F	CMOS RAM Checksum	44	A20 Gate
10	CPU Protected Mode	50	Initialize Interrupt Table
11	Display Configuration	51	Enable Timer Interrupt
12	Display Controller	60	Flexible (Floppy) Controller/Drive
13	Primary Display Error	61	Fixed (Hard) Disk Controller
14	Extended DMOS Test	62	Initialize Flexible (Floppy) Drives
15	AT-Bus Reset	63	Initialize Fixed (Hard) Drives
16	Initialize Tiger-Register	70	Real Time Clock (RTC)
17	Exists Extension ROM	71	Set Real Time Clock
18	Internal Mem Address Test	72	Parallel Interfaces
19	Remap Memory	73	Serial Interfaces
1A	Interleave Mode	74	External ROMs
1B	Remap Shadow Memory	75	Numeric Coprocessor
1C	Setup MRAM	76	Enable Keyboard and RTC Interrupts (IRQ9)
1D	Expanded Memory	F0	Display System Message
1E	AT Memory Error	F1	ROM at E000H
1F	Internal Memory Error	F2	Boot from Floppy or Hard Disk
20	Minimum Complete	F3	Setup Program
21	DMA Controller 1	F4	Password Program
22	DMA Controller 2	FC	DRAM Type Detection
23	Timer 0	FD	CPU Register Test
24	Initialize Internal Controllers		

Version 3.0

Code	Meaning
01	CPU test 1: verify CPU status bits
02	Powerup check - Init motherboard and chipset with default values; Check 8042 buffer
03	Clear 8042 keyboard controller - send command AA, fail if status is not 2 output buffer full
04	Reset 8042 keyboard controller
05	Get 8042 keyboard controller manufacturing status

Code	Meaning
06	Init motherboard chipset; disable color/mono video, 8237 DMA controller; reset 80x87; initialize 8255 timer 1; clear DMA/page registers/CMOS RAM shutdown byte
07	CPU test 2; read/write/verify CPU registers SS, SP, BP, with FF and 00
08	Initialize CMOS RAM/RTC
09	Checksum 32K of BIOS ROM
0A	Initialize video interface; initialize 6845 controller
0B	Test 8254 programmable interrupt timer channel 0
0C	Test 8254 programmable interrupt timer channel 1
0D	Test 8254 programmable interrupt timer channel 2
0E	Test CMOS RAM shutdown byte
0F	Test extended CMOS RAM, if present
10	Test 8237 DMA controller channel 0
11	Test 8237 DMA controller channel 1
12	Test 8237 DMA controller page registers
13	Test 8741 keyboard controller interface
14	Test memory refresh toggle
15	Test first 64K of base memory
16	Set up interrupt tables in low memory
17	Set up video I/O operations
18	(1 beep) Test MDA/CGA video memory unless EGA/VGA adapter is found
19	Test 8259 programmable interrupt timer channel 1
1A	Test 8259 programmable interrupt timer channel 0
1B	Test CMOS RAM battery level
1C	Test CMOS RAM checksum
1D	Set system memory size parameters
1E	Size base memory 64K at a time
1F	Test base memory found from 64K to 640K
20	Test stuck bit in 8259 programmable interrupt controller
21	Test for stuck NMI bits
22	Test 8259 programmable interrupt controller functionality
23	Test protected mode
24	Size extended memory above 1MB
25	Test all base and extended memory found, except the first 64K
26	Test protected mode exceptions
27	Init shadow RAM and move system BIOS and/or video BIOS into it if enabled by CMOS setup
28	Detect and initialize Intel 8242/8248 chip
2A	Detect and initialize keyboard
2B	Detect and initialize floppy drive
2C	Detect and initialize serial ports
2D	Detect and initialize parallel ports
2E	Detect and initialize hard drive
2F	Detect and initialize coprocessor
30	Reserved
31	Detect and initialize adapter ROMs
BD	Initialize Orvonton cache controller, if present
CA	Initialize 386 Micronics cache, if present
CC	Shutdown NMI handler
EE	Test for unexpected processor exception
FF	Interrupt 19 boot loader

Version 3.00-3.03 8/26/87 286 N3.03 Extensions

Code	Meaning
01	CPU test 1
02	Determine type of POST test
03	Clear 8042 keyboard controller
04	Reset 8042 keyboard controller
05	Get 8042 keyboard controller manufacturing status
06	Initialize LSI onboard chips
07	CPU test 2
08	Initialize CMOS RAM/RTC
09	Checksum 32K of BIOS ROM
0A	Initialize video interface
0B	Test 8254 programmable interrupt timer channel 0
0C	Test 8254 programmable interrupt timer channel 1
0D	Test 8254 programmable interrupt timer channel 2
0E	Test CMOS date and timer
0F	Test CMOS shutdown byte
10	Test DMA controller channel 0
11	Test DMA controller channel 1
12	Test DMA controller page registers
13	Test 8741 keyboard controller interface
14	Test memory refresh toggle
15	Test first 64K of base memory
16	Set up interrupt tables
17	Set up video I/O
18	Test video memory
19	Test 8259 programmable interrupt controller channel 1 mask bits
1A	Test 8259 programmable interrupt controller channel 2 mask bits
1B	Test CMOS battery level
1C	Test CMOS checksum
1D	Setup configuration byte for CMOS
1E	Sizing system memory & compare with CMOS
1F	Test found system memory
20	Test stuck 8259's interrupt bits
21	Test for stuck NMI bits
22	Test 8259 programmable interrupt controller functionality
23	Test protected mode and A20 gate
24	Size extended memory above 1MB
25	Test found system/extended memory
26	Test protected mode exceptions
2A	Detect and initialize keyboard
2B	Detect and initialize floppy drive
2C	Detect and initialize serial ports
2D	Detect and initialize parallel ports
2E	Detect and initialize hard drive
2F	Detect and initialize coprocessor
30	Test for unexpected processor exception
CC	POST_NMI

XT 8088/86 v3.1

Code	Meaning
01	CPU test 1
02	Determine type of POST test
06	Initialize 8259 programmable interrupt controller and 8237 DMA controller chips
07	CPU test 2
09	Checksum 32K of BIOS ROM
0A	Initialize video controller 6845 registers
15	Test first 64K of base memory
16	Set up interrupt tables
17	Set up video I/O
18	Test video memory
19	Test 8259 programmable interrupt controller channel 1 mask bits
1A	Test 8259 programmable interrupt controller channel 2 mask bits
1D	Setup configuration byte for CMOS
1E	Sizing system memory & compare with CMOS
1F	Test found system memory
20	Test stuck 8259's interrupt bits
21	Test for stuck NMI bits
22	Test 8259 programmable interrupt controller functionality
2A	Detect and initialize keyboard
2B	Detect and initialize floppy drive
2C	Detect and initialize serial ports
2D	Detect and initialize parallel ports
2E	Detect and initialize hard drive
2F	Detect and initialize coprocessor
31	Initialize option ROM's
FF	Interrupt 19 boot loader

386 v3.1

Code	Meaning	Code	Meaning
01	CPU test 1	1B	Test CMOS battery level
02	Determine type of POST test	1C	Test CMOS checksum data at 2E and 2Fh
03	Clear 8042 keyboard controller	1D	Configuration of CMOS if checksum good
04	Reset 8042 keyboard controller	1E	Sizing memory & compare with CMOS
05	Get 8042 keyboard controller status	1F	Tests memory from 64K to top of memory
06	Initialize LSI onboard chips	20	Test stuck 8259's interrupt bits
07	CPU test 2	21	Test for stuck NMI bits
08	Initialize CMOS RAM/RTC	22	Test 8259 PIC functionality
09	Checksum 32K of BIOS ROM	23	Test protected mode and A20 gate
0A	Initialize video interface	24	Size extended memory above 1MB
0B	Test 8254 PIC timer channel 0	25	Test extended memory with virtual 8086 mode and writing FFFF/AA55/0000 pattern
0C	Test 8254 PIC timer channel 1	26	Test protected mode exceptions
0D	Test 8254 PIC timer channel 2	27	Test cache controller or shadow RAM
0E	Test CMOS shutdown byte	28	Set up cache controller or 8042 controller
0F	Test extended CMOS	2A	Detect and initialize keyboard

Code	Meaning	Code	Meaning
10	Test DMA controller channel 0	2B	Detect and initialize floppy drive
11	Test DMA controller channel 1	2C	Detect and initialize serial ports
12	Test DMA controller page registers	2D	Detect and initialize parallel ports
13	Test 8741 keyboard controller interface	2E	Detect and initialize hard drive
14	Test memory refresh toggle	2F	Detect and initialize coprocessor
15	Test first 64K of base memory	31	Detect and initialize option ROMs
16	Set up interrupt tables	3B	Init sec cache with Opti chipset (486 only)
17	Set up video I/O	CC	NMI handler shutdown
18	Test video memory	EE	Test for unexpected processor exception
19	Test 8259 PIC channel 1 mask bits	FF	Interrupt 19 boot loader
1A	Test 8259 PIC channel 2 mask bits		

ISA/EISA v4.0

Code	Meaning	Code	Meaning
01	CPU test 1	4E	If POST loop pin set, reboot, otherwise display non-fatal error messages
02	CPU test 2	4F	Security check
03	Calculate BIOS EPROM	50	Write all CMOS values back to CMOS RAM
04	Test CMOS RAM interface	51	Preboot enabled
05	Initialize chipset	52	Initialize ROMs between C80000-EFFFF
06	Test memory refresh	53	Initialize time value at address 40 of BIOS
07	Setup low memory	55	Initialize DDNIL counter to NULL's
08	Setup interrupt vector table	63	Boot attempt
09	Test CMOS RAM checksum & load default	B0	Spurious interrupt in protected mode
0A	Initialize keyboard	B1	Unclaimed NMI
0B	Initialize video interface	BF	Program chipset
0C	Test video memory	C0	OEM specific
0D	OEM specific; init motherboard chips	C1	OEM specific
0F	Test DMA controller 0	C2	OEM specific
10	Test DMA controller 1	C3	OEM specific
11	DMA page registers	C4	OEM specific
14	Test 8254 timer 0 counter 2	C5	OEM specific
15	Verify 8259 PIC channel 1	C6	OEM specific
16	Verify 8259 PIC channel 2	C7	OEM specific
17	Test for stuck 8259 interrupt bits	C8	OEM specific
18	T Test 8259 functionality	C9	OEM specific
19	Test for NMI bits	D0	Debug
1F	Set EISA mode	D1	Debug
20	Initialize and enable EISA slot 0	D2	Debug
21	Initialize and enable EISA slot 1	D3	Debug
22	Initialize and enable EISA slot 2	D4	Debug
23	Initialize and enable EISA slot 3	D5	Debug
24	Initialize and enable EISA slot 4	D6	Debug
25	Initialize and enable EISA slot 5	D7	Debug
26	Initialize and enable EISA slot 6	D8	Debug
27	Initialize and enable EISA slot 7	D9	Debug
28	Initialize and enable EISA slot 8	DA	Debug
29	Initialize and enable EISA slot 9	DB	Debug

Code	Meaning	Code	Meaning
2A	Initialize and enable EISA slot 10	DC	Debug
2B	Initialize and enable EISA slot 11	DD	Debug
2C	Initialize and enable EISA slot 12	DE	Debug
2D	Initialize and enable EISA slot 13	DF	Debug
2E	Initialize and enable EISA slot 14	E1	Setup page 1
2F	Initialize and enable EISA slot 15	E2	Setup page 2
30	Size base memory from 256-640K and test	E3	Setup page 3
31	Test extended memory	E4	Setup page 4
32	If EISA mode flag set, test memory found during slot initialization	E5	Setup page 5
3C	Verify CPU switch in and out of protected, virtual 86 and 8086 page modes	E6	Setup page 6
3D	Check for mouse and initialize if present	E7	Setup page 7
3E	Initialize cache controller	E8	Setup page 8
3F	Enable shadow RAM	E9	Setup page 9
41	Initialize floppy drive controller and drives	EA	Setup page 10
42	Initialize hard drive controller and drives	EB	Setup page 11
43	Serial ports detected and initialized	EC	Setup page 12
44	Parallel ports detected and initialized	ED	Setup page 13
45	Coprocessor detected and initialized	EE	Setup page 14
46	Setup message print to screen	EF	Setup page 15
47	Boot speed set	FF	Boot via interrupt 19 if no errors detected

EISA BIOS

Code	Meaning	Code	Meaning
01	CPU Flags	2D	Initialize and enable EISA slot 13
02	CPU Registers	2E	Initialize and enable EISA slot 14
03	Initialize DMA	2F	Initialize and enable EISA slot 15
04	Memory refresh	30	Memory size 256K
05	Keyboard initialization	31	Memory test over 256K
06	ROM checksum	32	EISA memory
07	CMOS	3C	CMOS setup on
08	256K memory	3D	Mouse
09	Cache	3E	Cache RAM
0A	Set interrupt table	3F	Shadow RAM
0B	CMOS checksum	41	Initialize floppy drive controller and drives
0C	Keyboard initialization	42	Initialize hard drive controller and drives
0D	Video adapter	43	Serial ports detected and initialized
0E	Video memory	45	Coprocessor detected and initialized
0F	Test DMA controller 0	47	Boot speed set
10	Test DMA controller 1	4E	Manufacturing loop
11	DMA page registers	4F	Security check
14	Timer chip	50	Write all CMOS values back to CMOS RAM
15	Programmable interrupt controller 1	51	Enable NMI
16	Programmable interrupt controller 2	52	Adapter ROMs
17	Programmable interrupt controller stuck bits	53	Initialize time value at address 40 of BIOS
18	PIC maskable IRQs	63	Boot attempt
19	NMI bit check	B0	NMI in protected mode

Code	Meaning	Code	Meaning
1F	CMOS RAM	B1	Disable NMI
20	Initialize and enable EISA slot 0	BF	Program chipset
21	Initialize and enable EISA slot 1	C0	Cache on/off
22	Initialize and enable EISA slot 2	C1	Memory size
23	Initialize and enable EISA slot 3	C2	Base 256K test
24	Initialize and enable EISA slot 4	C3	DRAM page select
25	Initialize and enable EISA slot 5	C4	Video switch
26	Initialize and enable EISA slot 6	C5	Shadow RAM
27	Initialize and enable EISA slot 7	C6	Cache program
28	Initialize and enable EISA slot 8	C8	Speed switch
29	Initialize and enable EISA slot 9	C9	Shadow RAM
2A	Initialize and enable EISA slot 10	CA	OEM chipset
2B	Initialize and enable EISA slot 11	FF	Boot via interrupt 19 if no errors detected
2C	Initialize and enable EISA slot 12		

AWARD

The general procedures below are valid for greater than XT v3.0 and AT v3.02-4.2. The sequence may vary slightly between versions. If a failure occurs between 6- FF (unless it causes the computer to hang in the test), the system will keep outputting the POST sequence to the defined POST port. A normal error message will then be displayed on the screen when video is available. EISA codes typically go to 300h. ISA codes to 80h.

Award Test Sequence-up to v4.2

Procedure	Meaning
CPU	BIOS sets verifies and resets the error flags in the CPU (i.e. carry; sign; zero; stack overflow). Failure here is normally due to the CPU or system clock.
POST Determination	BIOS determines whether motherboard is set for normal operation or a continuous loop of POST (for testing). If the POST test is cycled 1-5 times over and over either the jumper for this function is set to burn-in or the circuitry involved has failed.
Keyboard Controller	BIOS tests internal operations of the keyboard controller chip (8042). Failure here is normally due to the keyboard chip.
Burn In Status	1-5 will repeat if the motherboard is set to burn in (you will see the reset light on all the time). If you haven't set the board for burn-in mode, there is a short in the circuitry.
Initialise Chipset	BIOS clears all DMA registers and CMOS status bytes 0E & 0F. BIOS then initialises 8254 (timer). Failure of this test is probably due to the timer chip.
CPU	A bit-pattern is used to verify the functioning of the CPU registers. Failure here is normally down to the CPU or clock chip.
RTC	Verifies that the real time clock is updating CMOS at normal intervals. Failure is normally the CMOS/RTC or the battery.
ROM BIOS Checksum	BIOS performs a checksum of itself against a predetermined value that will equal 00. Failure is down to the ROM BIOS.
Initialise Video	BIOS tests and initialises the video controller. Failure is normally the video controller (6845) or an improper setting of the motherboard or CMOS.
PIT	BIOS tests channels 0 1 2 in sequence. Failure is normally the PIT chip (8254/53).
CMOS Status	Walking-bit pattern tests CMOS shutdown status byte 0F. Failure normally in CMOS.

Procedure	Meaning
Extended CMOS	BIOS checks for extended information of chipset and stores it in the extended RAM area. Failure is normally due to invalid information and can be corrected by setting CMOS defaults. Further failure indicates either the chipset or the CMOS RAM.
DMA	Channels 0 and 1 are tested together with the page registers of the DMA controller chip(s)-8237. Failure is normally due to the DMA chips.
Keyboard	The 8042 keyboard controller is tested for functionality and for proper interfacing functions. Failure is normally due to the 8042 chip.
Refresh	Memory refresh is tested; the standard refresh period is 120-140 ns. Failure is normally the PIT chip in ATs or the DMA chip in XTs.
Memory	The first 64K of memory is tested with walking-bit patterns. Failure is normally due to the first bank of RAM or a data line.
Interrupt Vectors	BIOS interrupt vector table loaded to first bank of RAM. Failure here is not likely since memory in this area has been tested. If a failure does occur suspect the BIOS or the PIC.
Video ROM	Video ROM is initialised which performs an internal diagnostic before returning control to the System BIOS. Failure is normally the video adapter or the BIOS.
Video Memory	This is tested with a bit-pattern. This is bypassed if there is a ROM on the video adapter. Failure is normally down to the memory on the adapter.
PIC	Functionality of interrupt controller chip(s) is tested (8259). Failure is normally down to the 8259 chips but may be the clock.
CMOS Battery	BIOS verifies CMOS byte 0D is set which indicates CMOS battery power. Suspect the battery first and the CMOS second.
CMOS Checksum	A checksum is performed on the CMOS. Failure is either incorrect setup or CMOS chip or battery. If the test is passed the information is used to configure the system.
Determine System Memory	Memory up to 640K is addressed in 64K blocks. Failure is normally due to an address line or DMA chip. If all of the memory is not found there is a bad RAM chip or address line in the 64K block above the amount found.
Memory Test	Tests are performed on any memory found and there will normally be a message with the hex address of any failing bit displayed at the end of boot.
PIC	Further testing is done on the 8259 chips.
CPU protected mode	Processor is placed into protected mode and back into real mode; the 8042 is used for this. In case of failure suspect the 8042; CPU; CMOS; or BIOS in that order.
Determine Extended Memory	Memory above 1 Mb is addressed in 64K blocks. The entire block will be inactive if there is a bad RAM chip on a block.
Test Extended Memory	Extended memory is tested with a series of patterns. Failure is normally down to a RAM chip, and the hex address of the failed bit should be displayed.
Unexpected Exceptions	BIOS checks for unexpected exceptions in protected mode. Failure is likely to be a TSR or intermittent RAM failure.
Shadow/ Cache	Shadow RAM and cache activated; failure may be cache controller or chips. Check CMOS first for invalid information.
8242 Detection	BIOS checks for Intel 8242 keyboard controller and initialises. Failure may be an improper jumper setting or the 8242.
Initialise Keyboard	Failure could be the keyboard or the controller.
Initialise Floppy	All those set in the CMOS. Failure could be incorrect setup or controller or the drive.
Detect Serial Ports	BIOS searches for and initialises up to 4 serial ports at 3F8/2F8/3E8 and 2E8. Detection failure is normally due to an incorrect jumper setting somewhere or an adapter failure.
Detect Parallel Ports	BIOS searches for and initialises up to four parallel ports at 378/3BC and 278. Detection failure is normally due to an incorrect jumper setting somewhere or an adapter failure.
Initialise Hard Drive	BIOS initialises any hard drive set in CMOS. Failure could be due to invalid CMOS setup, hard drive or controller.
Detect NPU Coprocessor	Initialisation of any NPU Coprocessor found. Failure is due to either an invalid CMOS setup or the NPU is failing.
Initialise Adapter ROM	Any adapter ROMs between C800 and EFFF are initialised. The ROM will do an internal test before giving back control to the System ROM. Failure is normally due to the adapter ROM or the attached hardware.

Procedure	Meaning
Initialise External Cache	Any cache external to the 486 is enabled. Failure would indicate invalid CMOS setup, cache controller or chips.
NMI Unexpected Exceptions	A final check for unexpected exceptions before giving control to the Int 19 boot loader. Failure is normally due to a memory parity error or an adapter.
Boot Errors	Failure when the BIOS attempts to boot off the default drive set in CMOS is normally due to an invalid CMOS drive setup or as given by an error message. If the system hangs there is an error in the Master Boot Record or the Volume Boot Record.

Award Test Sequence-after v4.2 (386/486)

Procedure	Meaning
CPU	BIOS sets verifies and resets the error flags in the CPU then performs a register test by writing and reading bit patterns. Failure is normally due to the CPU or clock chip.
Initialise Support Chips	Video is disabled as is parity/DMA and NMI. Then the PIT/PIC and DMA chips are initialised. Failure is normally down to the PIT or DMA chips.
Init Keyboard	Keyboard and Controller are initialised.
ROM BIOS Test	A checksum is performed by the ROM BIOS on the data within itself and is compared to a preset value of 00. Failure is normally due to the ROM BIOS.
CMOS Test	A test of the CMOS chip which should also detect a bad battery. Failure is due to either the CMOS chip or the battery.
Memory Test	First 356K of memory tested with any routines in the chipsets. Failure normally due to defective memory.
Cache Initialisation	Any cache external to the chipset is activated. Failure is normally due to the cache controller or chips.
Initialise Vector Table	Interrupt vectors are initialised and the interrupt table is installed into low memory. Failure is normally down to the BIOS or low memory.
CMOS RAM	CMOS RAM checksum tested, BIOS defaults loaded if invalid. Check CMOS RAM.
Keyboard Init	Keyboard initialised and Num Lock set On. Check the keyboard or controller.
Video Test	Video adapter tested and initialised.
Video Memory	Tested on Mono and CGA adapters. Check the adapter card.
DMA Test	DMA controllers and page registers are tested. Check the DMA chips.
PIC Tests	8259 PIC chips are tested.
EISA Mode Test	A checksum is performed on the extended data area of CMOS where EISA information is stored. If passed the EISA adapter is initialised.
Enable Slots	Slots 0-15 for EISA adapters are enabled if the above test is passed.
Memory Size	Memory addresses above 265K written to in 64K blocks and addresses found are initialised. If a bit is bad, entire block containing it and those above will not be seen
Memory Test	Read/Write tests performed to memory over 256K; failure due to bad bit in RAM.
EISA Memory	Memory tests on any adapters initialised previously. Check the memory chips.
Mouse Initialisation	Checks for a mouse and installs the appropriate interrupt vectors if one is found. Check the mouse adapter if you get a problem.
Cache Init	The cache controller is initialised if present.
Shadow RAM Setup	Any Shadow RAM present according to the CMOS Setup is enabled.
Floppy Test	Test and initialise floppy controller and drive.
Hard Drive Test	Test and initialise hard disk controller and drive. You may have an improper setup or a bad controller or hard drive.
Serial/Parallel	Any serial/parallel ports found at the proper locations are initialised.
Maths Copro	Initialised if found. Check the CMOS Setup or the chip.
Boot Speed	Set the default speed at which the computer boots.
POST Loop	Reboot occurs if the loop pin is set; for manufacturing purposes.
Security	Ask for password if one has been installed. If not check the CMOS data or the chip.

Procedure	Meaning
Write CMOS	The BIOS is waiting to write the CMOS values from Setup to CMOS RAM. Failure is normally due to an invalid CMOS configuration.
Pre-Boot	BIOS is waiting to write the CMOS values from Setup to CMOS RAM.
Adapter ROM Initialise	Adapter ROMs between C800 and EFFF are initialised. The ROM will do an internal test before giving back control to the System ROM. Failure is normally due to the adapter ROM or the attached hardware.
Set Up Time	Set CMOS time to the value located at 40h of the BIOS data area.
Boot System	Control is given to the Int 19 boot loader.

3.Ox

Uses IBM beep patterns. Version 3.xx sends codes 1-24 to port 80 and 300 and the system hangs up. Afterwards, codes are sent to the POST port and screen without hanging up.

Code	Meaning
01	CPU test 1: verify CPU status bits
02	Powerup check-Wait for chips to come up; initialize motherboard and chipset (if present) with defaults. Read 8042 status and fail if its input buffer contains data but output buffer does not.
03	Clear 8042 interface-send self-test command AA, fail if status not 2 output buffer full.
04	Reset 8042 Keyboard controller-fail if no data input (status not equal 1) within a million tries, or if input data is not 55 in response to POST 03.
05	Get 8042 manufacturing status-read video type and POST type bits from 8042 discrete input port; test for POST type = manufacturing test or normal; fail if no response from 8042.
06	Initialize on-board chips-disable colour & mono video, parity, and 8237 DMA; reset 80x87 math chip, initialize 8255 timer 1, clear DMA chip and page registers and CMOS RAM shutdown byte: initialize motherboard chipset.
07	CPU test 2: read/write/verify registers except SS, SP, BP with FF and 00 data
08	Initialize CMOS RAM/RTC chip-update timer cycle normally; disable PIE, AIE, UIE and square wave. Set BCD date and 24-hour mode.
09	Checksum 32K of BIOS ROM; fail if not 0
0A	Initialize video interface-read video type from 8042 discrete input port. Fail if can't read it. Initialize 6845 controller register at either colour or mono adapter port to 80 columns, 25 rows, 8/14 scan lines per row, cursor lines at 6/11 (first) & 7/12 (last), offset to 0.
0B	Test 8254 timer channel 0- this test is skipped; already initialized for mode 3.
0C	Test 8254 timer channel 1-this test is skipped; already initialized for mode 0.
0D	Test 8254 timer channel 2-write/read/verify FF, then 00 to timer registers; ini with 500h for normal ops.
0E	Test CMOS RAM shutdown byte (3.03: CMOS date and timer-this test is skipped and functions performed
0F	Test extended CMOS RAM if present (3.03: test CMOS shutdown byte-write/read/verify a walk-to-left I pattern at CMOS RAM address 8F)
10	Test 8237 DMA controller ch 0-write/read/verify pattern AA, 55, FF and 00.
11	Test 8237 DMA controller ch 1-write/read/verify pattern AA, 55, FF and 00.
12	Test 8237 DMA controller page registers-write/read/verify pattern AA, 55, FF and 00: use port addresses to check out address circuitry to select page registers. At this point, POST enables user reboot.
13	Test 8741 keyboard controller interface-read 8042 status, verify buffers are empty, send AA self-test command, verify 55 response, send 8741 write command to 8042, wait for 8042 acknowledgement, send 44 data for 8741 (keyboard enabled, system flag, AT interface), wait for ack, send keyboard disable command, wait for ack. Fail if no ack or improper responses.
14	Test memory refresh toggle circuits-fail if not toggling high and low.
15	Test first 64K of base memory-disable parity checking, zero memory, 64K at a time, to clear parity errors, enable parity checking, write/read/verify 00, 5A, FF and A5 at each address.
16	Set up interrupt vector tables in low memory.

Code	Meaning
17	Set up video I/O operations-read 8042 (motherboard switch or jumper) to find whether colour or mono adapter installed; validate by writing a pattern to mono memory B0000 and select mono I/O port if OK or colour if not, and initialize it via setting up the hardware byte and issuing INT 10. Then search for special video adapter BIOS ROM at C0000 (EGA/VGA), and call it to initialize if found. Fail if no 8042 response.
18, 1 beep	Test MDA/CGA video memory unless EGA/VGA adapter is found-disable video, detect mono video RAM at B0000 or colour at B8000, write/read/verify test it with pattern A5A5, fill it with normal attribute, enable the video card. No error halt unless enabled by CMOS. Beep once to let user know first phase of testing complete. From now on, POST will display test and error messages on screen.
19	Test 8259 PIC mask bits, channel 1-write/read/verify 00 to mask register.
1A	Test 8259 PIC mask bits, channel 2-write/read/verify 00 to mask register.
1B	Test CMOS RAM battery level-poll CMOS RTC/RAM chip for battery level status. Display error if level is low, but do not halt.
1C	Test CMOS RAM checksum-check battery level again, calculate checksum of normal and extended CMOS RAM. Halt if low battery or checksum not 0; otherwise reinitialize motherboard chipset if necessary.
1D	Set system memory size parameters from CMOS RAM data, Cannot fail.
1E	Size base memory 64K at a time, and save in CMOS. Cannot fail, but saves diagnostic byte in CMOS RAM if different from size in CMOS.
1F	Test base memory found from 64K to 640K-write/read/verify FFAA and 5500 patterns by byte. Display shows failing address and data.
20	Test stuck bits in 8259 PICs
21	Test for stuck NMI bits (parity /I0 check)
22	Test 8259 PIC interrupt functionality-set up counter timer 0 to count down and issue an interrupt on IRQ8. Fail if interrupt does not occur.
23	Test protected mode, A20 gate. and (386 only) virtual 86 & 8086 page mode.
24	Size extended memory above 1Mb; save into CMOS RAM. Cannot fail, but saves diagnostic byte in CMOS RAM if different from CMOS.
25	Test all base and extended memory found (except the first 64K) up to 16 Mb. Disable parity check but monitor for parity errors. Write/read/verify AA55 then 55AA pattern 64K at a time. On 386 systems use virtual 8086 mode paging system. Displays actual and expected data and failing address.
26	Test protected mode exceptions-creates the circumstances to cause exceptions and verifies they happen; out-of-bounds instruction, invalid opcode, invalid TSS (JMP, CALL, IRET, INT), segment not present on segment register instruction, generate memory reference fault by writing to a read-only segment.
27	Initialise shadow RAM and move system BIOS and/or video BIOS into it if enabled by setup. Also (386 only) initialise the cache controller if present in system. This is not implemented in some versions of 3.03
28	Detect and initialise Intel 8242/8248 chip (not implemented in 3.03)
29	Reserved
2A	Initialise keyboard
2B	Detect and initialise floppy drive
2C	Detect and initialise serial ports
2D	Detect and initialise parallel ports
2E	Detect and initialise hard drive
2F	Detect and initialise math coprocessor
30	Reserved
31	Detect and initialise adapter ROMs
BD	Initialize Orvonton cache controller if present
CA	Initialize 386 Micronics cache if present
CC	Shutdown NMI handler
EE	Test for unexpected processor exception
FF	INT 19 boot

3.00-3.03 8/26/87

Code	Meaning
01	Processor test part 1; Processor status verification. Tests following CPU status flags: set/clear carry zero sign and overflow (fatal). Output: infinite loop if failed; continue test if OK. Registers: AX/BP.
02	Determine POST test. Manufacturing (e.g. 01-05 in loop) or normal (boot when POST finished). Fails if keyboard interface buffer filled with data. Output: infinite loop if failed; continue if OK. Registers: AX/BX/BP.
03	Clear 8042 keyboard interface. Send verify TEST_KBRD command (AAh). Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
04	Reset 8042 keyboard controller. Verify AAh return from 03. Infinite loop if test fails.
05	Get 8042 keyboard controller manufacturing status. Read input port via keyboard controller to determine manufacturing or normal mode operation. Reset system if manufacturing status from 02. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
06	Init chips on board LSI chips. Disable colour/mono video; parity and DMA (8237A). Reset coprocessor; initialise (8254) timer 1; clear DMA page registers and CMOS shutdown byte.
07	Processor test #2. read/write verify SS/SP/BP registers with FFh and 00h data pattern.
08	Initialize CMOS chip
09	EPROM checksum for 32 Kbytes
0A	Initialize video interface
0B	Test 8254 channel 0
0C	Test 8254 channel 1
0D	Test 8254 channel 2
0E	Test CMOS date and timer
0F	Test CMOS shutdown byte
10	Test DMA channel 0
11	Test DMA channel 1
12	Test DMA page registers
13	Test 8741 keyboard controller
14	Test memory refresh toggle circuits
15	Test 1st 64k bytes of system memory
16	Setup interrupt vector table
17	Setup video I/O operations
18	Test video memory
19	Test 8259 channel 1 mask bits
1A	Test 8259 channel 2 mask bits
1B	Test CMOS battery level
1C	Test CMOS checksum
1D	Setup configuration byte from CMOS
1E	Sizing system memory & compare w/CMOS
1F	Test found system memory
20	Test stuck 8259'S interrupt bits
21	Test stuck NMI (parity/IO chk) bits
22	Test 8259 interrupt functionality
23	Test protected mode and A20 gate
24	Sizing extended memory above 1MB
25	Test found system/extended memory
26	Test exceptions in protected mode

286 N3.03 Extensions

Code	Meaning
2A	POST_KEYBOARD present during reset keyboard before boot has no relationship to POST 19.
2B	POST_FLOPPY present during init of floppy controller and drive(s)
2C	POST_COMM present during init of serial cards.
2D	POST_PRN present during init of parallel cards
2E	POST_DISK present during init of hard disk controller and drive(s)
2F	POST_MATH present during init of coprocessor. Result remains after DOS boot; left on the port 80 display
30	POST_EXCEPTION present during protected mode access or when processor exceptions occur. A failure indicates that protected mode return was not possible
CC	POST_NMI present when selecting the F2 system halt option

Original XT

Code	Meaning	Code	Meaning
03	Flag resister test	30	V40 DMA if present
06	CPU register test	33	Verify system clock initialization
09	System hardware initialization	36	Keyboard test
0C	BIOS checksum	39	Setup interrupt table
0F	DMA page register initialization	3C	Read system configuration switches
12	Test DMA address and count registers	3F	Video test
15	DMA initialization	42	Serial port determination
18	Timer test	45	Parallel port determination
1B	Timer initialization	48	Game port determination
1E	Start RAM initialization	4B	Copyright message display
21	Test base 64K of RAM	4E	Calculation of CPU speed
24	Setup init. and temp stack	54	Test of system memory
27	Initialize PIC	55	Floppy drive test
2A	Interrupt mask register test	57	System initialized before boot
2D	Hot interrupt test	5A	Call to Int 19

XT 8088/86 BIOS v3.1

Code	Meaning
01	Processor test 1; processor status verification. Tests the following processor status flags, carry, zero, sign, overflow. The BIOS will set each flags, verify they are set, then turn each flag off and verify it is off. Failure of any flag will cause a fatal error.
02	Determine type of POST test, manufacturing or normal, which can be set by a jumper on some motherboards. If the status is normal, POST continues through and, assuming no errors, boot is attempted. If manufacturing, POST will run in continuous loop and boot will not be attempted.Failed if keyboard interface buffer filled with data.
03	Clear 8042 Keyboard Controller-Test by sending TEST_KBRD command (AAh) and verifying controller reads command. Reset Keyboard Controller then verifiy controller returns Aah.
04	Get Manufacturing Status
05	The last test in the manufacturing cycle. If test 2 found the status to be manufacturing, this POST will trigger a reset and POSTs 1-5 will be repeated continuously.
06	Init 8259 PIC and 8237 DMA controller chips. Disable colour and mono video, parity circuits and DMA chips. Reset math coprocessor. Initialise 8253 Timer channel 1. Clear DMA chip and page registers.
07	Processor test #2. Write, read and verify all registers except SS, SP and BP with data patterns 00 and FF.

Code	Meaning
08	Initialize CMOS Timer. Update timer cycle normally
09	EPROM checksum for 32 Kbytes. Test failed if sum not equal to 0. Also checksums the sign-on message.
0A	Initialize video controller 6845 registers as follows: 25 lines x 80 columns, first cursor scan line at 6/11 and last at 7/12, reset display offset to 0.
0B	Test Timer (8254) Channel 0. These three timer tests verify that the 8254 timer chip is functioning properly.
0C	Test Timer (8254) Channel 1
0D	Test Timer (8254) Channel 2
0E	Test CMOS Shutdown Byte. Use walking bit (1) algorithm to check interface to CMOS circuit.
0F	Test Extended CMOS and Initialize CHIPSET. On motherboards with chip sets that support extended CMOS configurations, such as Chips and Technologies, the BIOS tables of CMOS information configure the chip set. These chip sets have an extended storage mechanism that allows you to save a system configuration after power is turned off. A checksum verifies the validity of the extended storage and, if valid, permits the information to be loaded into extended CMOS RAM.
10	Test DMA Channel 0. These 3 three functions initialize the DMA chip and then test it using an AA, 55, FF, 00 pattern. Port addresses are used to check the address circuit to DMA page registers.
11	Test DMA Channel 1. Test DMA Page Registers.
12	Test DMA Page Registers.
13	Test Keyboard Controller. Test keyboard controller interface.
14	Test Memory Refresh.
15	Test 1st 64K of system memory. An extensive parity test is performed on the first 64K of system memory. This memory is used by the BIOS
16	Setup interrupt vector table in 1st 64K
17	Setup video I/O operations. If a CGA or MDA adapter is installed, the video is initialized by the system BIOS. If the system BIOS detects an EGA or VGA adapter, the option ROM BIOS installed on the video adapter is used to initialize and set up the video.
18	Test video memory for CGA and MDA video boards. This is not performed by the system BIOS on EGA or VGA video adapters-the board's own EGA or VGA BIOS will ensure that it is functioning properly.
19	Test 8259 channel 1 mask bits. These two tests verify 8259 masked interrupts by alternately turning off and on the interrupt lines. Unsuccessful completion will generate a fatal error.
1A	Test 8259 channel 2 mask bits.
1B	Test CMOS Battery Level. Verifies that the battery status bit is set to ``1". A ``0" can indicate a bad battery or some other problem, such as bad CMOS.
1C	Set Configuration from CMOS. If the checksum is good, the values are used to configure the system.
1D	Test CMOS Checksum. This function tests the CMOS checksum data (located at 2Eh and 2Fh), and Extended CMOS checksum, if present, to be sure they are valid.
1E	Size System Memory. The system memory size is determined by writing to addresses from 0K to 640K, starting at 0 and continuing until an address does not respond. This tells the BIOS that this is the end of the memory. This value is then compared to the CMOS value to ensure they are the same. If they are different a flag is set and at the end of POST an error message is displayed.
1F	Test found system memory. Tests from 64K to the top of memory found by writing the pattern FFAA and 5500 then reading the pattern back, byte by byte, and verifying that it is correct
20	Test stuck 8259's interrupt bits
21	Test stuck NMI (parity/IO chk) bits
22	Test 8259 interrupt functionality
23	Test Protected Mode. Verifies protected mode, 8086 virtual mode as well as 8086 page mode. Protected mode ensures that any data about to be written to extended memory (above 1MB) is checked to ensure that it is suitable for storage there.
24	Size Extended Memory. This function sizes memory above 1MB by writing to addresses starting at 1MB and continuing to 16MB on 286 and 386SX systems and 64MB on 386 systems until there is no response. This determines the total extended memory, which is compared with CMOS to ensure the values are the same. If they are different a flag is set and at the end of POST an error message is displayed.
25	Test Found Extended Memory using virtual 8086 paging mode and writing an FFFF, AA55, 0000 pattern.
26	Test Protected Mode Exceptions.

Code	Meaning
27	Setup Cache Control or Shadow RAM. Tests for Shadow RAM (286, 386SX, 386, and 486) and cache controller (386 and 486 only) functionality. Systems with CGA and MDA adapters will indicate that Video Shadow RAM is enabled, even though there is no BIOS ROM to shadow. This is normal.
28	Setup 8242. Optional 8242/8248 Keyboard Controller detection and support.
29	Reserved.
2A	Initialise keyboard
2B	Initialise floppy controller and drive
2C	Initialise COM ports
2D	Initialised LPT ports
2E	Initialize Hard Drive & Controller.
2F	Initialise maths coprocessor
30	Reserved.
31	Initialise option ROMs
3B	Initialize Secondary Cache w/ OPTi chip set
FF	Int 19 Boot attempt

Modular (386) BIOS v3.1

Also for PC/XT v3.0+ and AT v3.02+. Tests do not necessarily execute in numerical order.

Code	Meaning
01	Processor test part 1. Processor status verification. Tests the following processor-status flags: set/clear carry; zero; sign and overflow (fatal). BIOS sets each flag; verifies they are set and turns each flag off verifying its state. Failure of a flag means a fatal error. Output: infinite loop if failed; continue test if OK. Registers: AX/BP.
02	Determine POST type; whether normal (boot when POST finished) or manufacturing (run 01-05 in loop) which is often set by a jumper on some motherboards. Fails if keyboard interface buffer filled with data. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
03	Clear 8042 keyboard interface. Send verify TEST_KBRD command (AAh). Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
04	Reset 8042 keyboard controller. Verify AAh return from 03. Infinite loop if test fails. Registers: AX/BX/BP.
05	Get 8042 keyboard controller manufacturing status; read input port via keyboard controller to determine manufacturing or normal mode operation. Reset system if manufacturing; i.e. if 02 found the status to be Manufacturing triggers a reset and 01-05 are repeated continuously. Output: infinite loop if failed; continue test if OK. Registers: AX/BX/BP.
06	Initialise chips on board LSI chips. Disables colour and mono video/parity circuits/DMA (8237) chips; resets maths copro; initialises timer 1 (8255); clears DMA chip and page registers and the CMOS shutdown byte.
07	Processor Test 2. Reads writes and verifies CPU registers except SS/SP/BP with data pattern FF and 00.
08	Initialises CMOS timer/RTC and updates timer cycle; normally CMOS (8254) timer; (8237A) DMA; (8259) interrupt and EPROM.
09	EPROM Checksum; test fails if not equal to 0. Also checksums sign-on message.
0A	Initialise Video Interface; specifically register 6845 to 80 characters per row and 25 rows per screen and 8/14 scan lines per row for mono/colour; first scan line of cursor 6/11; last scan line of cursor 7/12; reset display offset to 0.
0B	Test Timer (8254) Channel 0. See also below.
0C	Test Timer (8254) Channel 1.
0D	Test Timer (8254) Channel 2.
0E	Test CMOS Shutdown Byte using a walking-bit algorithm.
0F	Test Extended CMOS. On motherboards supporting extended CMOS configuration the BIOS tables of CMOS information configure the chipset which has an extended storage facility enabling you to keep the configuration with the power off. A checksum is used for verification.
10	Test DMA Channel 0. This and next two tests initialise the DMA chip and test it with an AA/55/FF/00 pattern. Port addresses used to check address circuit to DMA page circuit registers.

Code	Meaning
11	DMA Channel 1
12	DMA Page Registers
13	Test keyboard controller interface.
14	Test memory refresh toggle circuits.
15	First 64K of system memory which is used by the BIOS; an extensive parity test.
16	Interrupt Vector Table. Sets up and loads interrupt vector tables in memory for the 8259 PIC.
17	Video I/O operations. Initialises the video; EGA and VGA ROMs are used if present.
18	Video memory test for CGA and mono cards (EGA and VGA have their own procedures).
19	Test 8259 mask bits-Channel 1.Interrupt lines turned alternately off and on. Failure is fatal.
1A	8259 Mask Bits-Channel 2
1B	CMOS battery level; verifies battery status bit set to 1. 0 could indicate bad battery at CMOS.
1C	Tests the CMOS checksum data at 2E and 2Fh and extended CMOS checksum if present.
1D	Configuration of the system from CMOS values if the checksum is good.
1E	System memory size is determined by writing to addresses from 0-640K continuing till there is no response. The size is then compared to the CMOS and a flag set if they do not compare. An error message will then be displayed.
1F	Tests memory from the top of 64K to the top of memory found by writing patterns FFAA and 5500 and reading them back byte by byte
20	Stuck 8259 Interrupt Bits.
21	Stuck NMI bits (parity or I/O channel check).
22	8259 function.
23	Verifies protected mode; 8086 virtual and page mode.
24	As for 1E but for extended memory from 1-16Mb on 286/386SX systems and 64 Mb on 386s and above. The value found is compared to the CMOS settings.
25	Tests extended memory above using virtual 8086 paging mode and writing an FFFF/AA55/0000 pattern.
26	Protected Mode Exceptions; tests other aspects of protected mode operations.
27	Tests cache control (386/486) or Shadow RAM. Systems with CGA and MDA indicate that video shadow RAM is enabled even though there is no BIOS ROM to shadow.
28	Set up cache or 8242 keyboard controller. Optional Intel 8242/8248 controller detection and support.
29	Reserved.
2A	Initialise keyboard and controller.
2B	Initialise floppy drive(s) and controller.
2C	Detect and initialise serial ports.
2D	Detect and initialise parallel ports.
2E	Initialise hard drive and controller.
2F	Detect and initialise maths coprocessor.
30	Reserved.
31	Detect and initialise option ROMs. Initialises any between C800-EFFF.
3B	Initialise secondary cache with OPTi chipset (486 only).
CC	NMI Handler Shutdown. Detects untrapped NMIs during boot.
EE	Unexpected Processor Exception.
FF	Boot Attempt; if POST is complete and all components are initialised with no errors.

ISA/EISA BIOS v4.0

EISA codes may be sent to 300h.

Code	Meaning
01	Processor test 1: Verify CPU status flags-set, test, clear, and test the carry, zero, sign, overflow flags (fatal)
02	Processor test 2: Write/read/verify all CPU registers, except SS, SP and BP with data patterns FF and 00.

Code	Meaning
03	Calculate BIOS EPROM and sign-on message checksum; fail if not 0
04	Test CMOS RAM interface and verify battery power Is available.
05	Initialize chips: Disable NMI, PIE, AIE, UEI, SQWV; disable video, parity checking, and DMA: reset math coprocessor, clear all page registers and CMOS RAM shutdown byte: Initialize timers 0, 1 and 2, and set EISA timer to a known state: initialize DMA controllers 0 and 1: initialize interrupt controllers 0 and 1; initialise EISA extended registers.
06	Test memory refresh toggle to ensure memory chips can retain data.
07	Set up low memory; Initialize chipset early; test presence of memory; run OEM chipset initialization routines, clear lower 256K memory; enable parity checking and test in lower 256K; test lower 256K.
08	Setup interrupt vector table; initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00-1F according to INT_TBL.
09	Test CMOS RAM checksum and load default; if checksum is bad.
0A	Initialize keyboard; detect type of keyboard controller (optional); set NumLock status.
0B	Initialize video interface; read CMOS RAM location 14 to find out type of video in use; detect and initialise the video adapter.
0C	Test video memory; write signon message to screen.
0D	OEM specific-initialise motherboard special chips as required by OEM; initialise cache controller early, when cache is separate from chipset.
0F	Test DMA controller 0 with AA, 55, FF, 00 pattern.
10	Test DMA controller 1 with AA, 55, FF, 00 pattern.
11	DMA page registers-use 1/O ports to test address circuits.
14	Test 3254 timer 0 counter 2.
15	Verify 8259 interrupt controller channel 1 by toggling interrupt lines off/on.
16	Verify 8259 interrupt controller channel 2 by toggling interrupt lines off/on.
17	Test stuck 8259 interrupt bits: turn interrupt bits off and verify no interrupt mask register is on.
18	Test 8259 functionality: force an interrupt and verify the interrupt occurred.
19	Test stuck NMI bits (parity I/O check): verify NMI can be cleared.
1F	Set EISA mode: If EISA non-volatile memory checksum is good, execute EISA init. If not, execute ISA tests and clear EISA mode flat. Test EISA config mem checksum and communication ability.
20	Initialize and enable EISA slot 0 (system board).
21-2F	Initialize and enable EISA slots 1-15.
30	Size base memory from 256-640K and test with various patterns.
31	Test extended memory above 1Mb using various patterns. Press Esc to skip.
32	If EISA mode flag set, test EISA memory found during slot initialization. Skip this by pressing Esc.
3C	Verify CPU can switch in/out of protected, virtual 86 and 8086 page modes.
3D	Detect if mouse is present, initialize it, and install interrupt vectors.
3E	Initialize cache controller according to CMOS RAM setup
3F	Enable shadow RAM according to setup or if MEM TYPE is SYS in the EISA configuration information.
41	Initialise floppy disk drive controller and any drives.
42	Initialise hard disk drive controller and any drives.
43	Detect and initialise serial ports.
44	Detect and initialize parallel ports.
45	Detect and initialise math coprocessor
46	Print Setup message (press Ctrl-Alt-Esc to enter Setup at bottom of the screen, and enable setup.
47	Set speed for boot.
4E	Reboot if manufacturing POST loop pin is set. Otherwise, display messages for non-fatal POST errors; setup if user pressed Ctrl-Alt-Esc.
4F	Security check (optional): Ask for password.
50	Write all CMOS RAM values back to CMOS RAM, and clear the screen.
51	Preboot enable: Enable parity, NMI, cache before boot.
52	Initialize ROMs between C80000-EFFFF. When FSCAN enabled, init from C80000 to F7FFF.

Code	Meaning
53	Initialize time value at address 40 of BIOS RAM area.
55	Initialize DDNIL counter to NULLs.
63	Boot attempt: Set low stack and boot by calling INT 19.
88	CPU failed to initialise
B0	Spurious interrupt occurred in protected mode.
B1	Unclaimed NMI. If unmasked NMI occurs, display Press F1 to disable NMI, F2 to boot.
BF	Program chipset: Called by POST 7 to program chipset from CT table.
C0	OEM specific-Turn on/off cache.
C1	OEM specific-Test for memory presence and size on-board memory.
C2	OEM specific-Initialize board and turn on shadow and cache for fast boot.
C3	OEM specific-Turn on extended memory DRAM select and initialize RAM.
C4	OEM specific-Handle display/video switch to prevent display switch errors.
C5	OEM specific-Fast Gate A20 handling.
C6	OEM specific-Cache routine for setting regions that are cacheable.
C7	OEM specific-Shadow video/system BIOS after memory proven good.
C8	OEM specific-Handle special speed switching.
C9	OEM specific-Handle normal shadow RAM operations.
D0-DF	Debug: available POST codes for use during development.
E1-EF	Setup pages: E1 = page 1, E2 = page 2, etc.
FF	If no error flags such as memory size are set, boot via INT 19-load system from drive A, then C; display error message if boot device not found.

EISA BIOS

Code	Meanings	Code	Meaning
1	CPU flags	2D	Slot 13
2	CPU registers	2E	Slot 14
3	Initialise DMA	2F	Slot 15
4	Memory refresh	30	Memory size 256K
5	Keyboard initialisation	31	Memory test over 256K
06	ROM checksum	32	EISA memory
07	CMOS	3C	CMOS setup on
08	256K memory	3D	Mouse
09	Cache	3E	Cache RAM
0A	Set interrupt table	3F	Shadow RAM
0B	CMOS checksum	40	N/A
0C	Keyboard initialisation	41	Floppy drive
0D	Video adapter	42	Hard drive
0E	Video memory	43	RS232/parallel
0F	DMA channel 0	45	NPU
10	DMA channel 1	47	Speed
11	DMA page register	4E	Manufacturing loop
14	Timer chip	4F	Security
15	PIC controller 1	50	CMOS update
16	PIC controller 2	51	Enable NMI
17	PIC stuck bits	52	Adapter ROMs
18	PIC maskable IRQs	53	Set time
19	NMI bit check	63	Boot
1F	CMOS XRAM	B0	NMI in protected

Code	Meanings	Code	Meaning
20	Slot 0	B1	Disable NMI
21	Slot 1	BF	Chipset program
22	Slot 2	C0	Cache on/off
23	Slot 3	C1	Memory size
24	Slot 4	C2	Base 256K test
25	Slot 5	C3	DRAM page select
26	Slot 6	C4	Video switch
27	Slot 7	C5	Shadow RAM
28	Slot 8	C6	Cache program
29	Slot 9	C8	Speed switch
2A	Slot 10	C9	Shadow RAM
2B	Slot 11	CA	OEM chipset
2C	Slot 12	FF	Boot

4.5x-non PnP

Code	Meaning
C0	Turn Off Chipset Cache; OEM specific cache control
01	Processor Test 1; Status (1Flags) Verification. Tests carry/zero/sign/overflow processor status flags.
02	Processor Test 2; Read/Write/Verify CPU registers except SS/SP and BP with pattern FF and 00.
03	Initialise Chips; Disable NMI/PIE/UEL/SQWV; video; parity checking; DMA; reset maths coprocessor. Clear all page registers and CMOS shutdown byte. Initialise timer 0 1 and 2 including set EISA timer to a known state. Initialise DMA controllers 0 and 1; interrupt controllers 0 and 1 and EISA extended registers.
04	Test Memory Refresh Toggle
05	Blank video; initialise keyboard
06	Reserved
07	Test CMOS Interface and battery status. Detects bad battery. BE and Chipset Default Initialisation. Program chipset registers with power-on BIOS defaults.
C1	Memory Presence Test; OEM specific test to size on-board memory
C5	Early Shadow; OEM specific-enable for fast boot
C6	Cache Presence Test; External cache size detection
08	Setup Low Memory; Early chipset initialisation. Memory presence test. OEM chipset routines. Clear low 64K of memory. Test first 64K memory
09	Early Cache Initialisation. Cyrix CPU Initialisation. Cache Initialisation
0A	Setup Interrupt Vector Table; Initialise first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialise INT 00-FF according to INT_TBL.
0B	Test CMOS RAM Checksum if bad or Insert key depressed; load defaults.
0C	Initialise keyboard; Set NUM LOCK status.
0D	Initialise video interface; Detect CPU Clock. Read CMOS location 14h to find out type of video. Detect and initialise video adapter.
0E	Test Video Memory. Write signon message to screen. Set up Shadow RAM and enable as per Setup.
0F	Test DMA Controller 0. BIOS Checksum Test. keyboard detect and initialisation.
10	Test DMA Controller 1
11	Test DMA Page Registers
12-13	Reserved
14	Test Timer Counter 2. Test 8254 Timer 0 Counter 2
15	Test 8259-1 Mask Bits. Alternately turns on and off interrupt lines.
16	Test 8259-2 Mask Bits. Alternately turns on and off interrupt lines.
17	Test Stuck 8259 interrupt bits. Turn off interrupts then verify no interrupt mask register is on.
18	Test 8259 Interrupt Functionality. Force an interrupt and verify that it occurred.

Code	Meaning
19	Test Stuck NMI Bits (Parity/I/O check). Verify NMI can be cleared.
1A	Display CPU Clock
1B-1E	Reserved
1F	Set EISA Mode. If EISA NVR checksum is good execute EISA initialisation. If not execute ISA tests and clear EISA mode flag. Test EISA configuration memory integrity (checksum and communication interface).
20	Enable Slot 0. Motherboard
21-2F	Enable Slots 1-15
30	Size Base and Extended Memory. From 256-640K and that above 1 Mb.
31	Test Base and Extended Memory. Various patterns are used on that described above. This will be skipped in EISA mode and can be skipped in ISA mode with Esc.
32	Test EISA Extended Memory. If EISA Mode flag is set then test EISA memory found in slots initialisation. This will be skipped in ISA mode and can be skipped in EISA mode with Esc.
33-3B	Reserved
3C	Setup Enabled
3D	Initialise and Install Mouse
3E	Setup Cache Controller
3F	Reserved
BF	Chipset Initialisation. Program registers with Setup values.
40	Display virus protect enable or disable.
41	Initialise floppy drive(s) and controller
42	Initialise hard drive(s) and controller
43	Detect and initialise Serial/Parallel Ports and game port.
44	Reserved
45	Detect and Initialise Maths Coprocessor
46	Reserved
47	Reserved
48-4D	Reserved
4E	Manufacturing POST Loop or Display Messages. Reboot if manufacturing POST Loop Pin is set. Otherwise display any messages (i.e. non-fatal errors during POST) and enter Setup.
4F	Security Check. Ask password (optional)
50	Write CMOS. Write all CMOS values back to RAM and clear screen.
51	Pre-boot Enable. Enable Parity Checker; NMI and cache before boot.
52	Initialise Option ROMs. Between C800-EFFF. When FSCAN is enabled will initialise between C800-F7FF
53	Initialise Time Value In 40h BIOS area.
60	Setup Virus Protect. According to Setup
61	Set Boot Speed
62	Setup NumLock. According to Setup
63	Boot attempt. Set Low Stack. Boot via INT 19
88	CPU failed to initialise
B0	Spurious. If interrupt occurs in protected mode
B1	Unclaimed NMI. If unmasked NMI occurs display Press F1 to disable NMI; F2 reboot
E1-EF	Setup Pages. E1=Page 1; E2=Page 2 etc
FF	Boot

4-5x PnP Elite

Code	Meaning
C0	1.Turn off OEM specific cache, shadow 2.Initialize standard devices with default values: DMA controller (8237) Programmable Interrupt Controller (8259) Programmable Interval Timer (8254) RTC chip
C1	Auto detection of onboard DRAM & Cache
C3	1. Test the first 256K DRAM 2. Expand the compressed codes into temporary DRAM area including compressed BIOS & Option ROMs
C5	Copy BIOS from ROM into E000FFFF shadow RAM so that POST will go faster
01-02	Reserved
03	Initialize EISA registers (EISA BIOS only)
04	Reserved
05	1. Keyboard Controller Self Test 2. Enable Keyboard Interface
07	Verifies CMOS's basic R/W functionality
BE	Program defaults values into chipset according to the MODBINable Chipset Default Table
09	1.Program configuration register of Cyrix CPU according to the MODBINable Cyrix Register Table 2.OEM specific cache initialization
0A	1.Initialize the first 32 interrupt vectors with corresponding interrupt handlers. Initialize INT No from 33120 with Dummy (Spurious) interrupt handler 2.Issue CPUID instruction to identify CPU type 3.Early Power Management initialization (OEM specific)
0B	1.Verify the RTC time is valid or not 2.Detect bad battery 3.Read CMOS data into BIOS stack area 4.PnP init including (PnP BIOS only) . Assign CSN to PnP ISA card. Create resource map from ESCD 5.Assign IO & Memory for PCI devices (PCI BIOS only)
0C	Initialization of the BIOS data area (40:040:FF)
0D	1.Program some chipset's value according to setup.(Early setup value program). 2.Measure CPU speed for display & decide the system clock speed 3.Video initialization including Mono, CGA, EGA/VGAIf no display device found, the speaker will beep.
0E	1.Initialize the APIC (MultiProcessor BIOS only) 2.Test video RAM (If Monochrome display device found) 3.Show message including:Award logo Copyright string BIOS date code & Part No OEM specific sign on messages Energy Star logo (Green BIOS only) CPU brand, type & speed
0F	DMA channel 0 test
10	DMA channel 1 test
11	DMA page registers test
14	Test 8254 timer 0 counter 2
15	Test 8259 interrupt mask bits for channel 1
16	Test 8259 interrupt mask bits for channel 2
19	Test 8259 functionality
1E	If EISA NVM checksum is good, execute EISA initialization (EISA BIOS only)
30	Get base memory & extended memory size
31	1.Test base memory from 256K to 640K 2.Test extended memory from 1M to the top of memory
32	1.Display the Award Plug & Play BIOS extension message(PnP BIOS only) 2.Program all onboard super I/O chips(if any) including COM ports, LPT ports, FDD port according to setup
3C	Set flag to allow users to enter CMOS setup utility
3D	1.Initialise keyboard 2.Install PS2 mouse
3E	Try to turn on level 2 cache Note: Some chipset may need to turn on the L2 cache in this stage. But usually, the cache is turn on later in Post 61h

Code	Meaning
BF	1.Program the rest of the chipset's value according to setup (later setup value program) 2.If auto configuration is enabled, programmed the chipset with predefined values in the MODBINable AutoTable
41	Initialize floppy disk drive controller
42	Initialize hard drive controller
43	If it is a PnP BIOS, initialize serial & parallel ports
45	Initialize math coprocessor
4E	If there is any error detected (such as video, KB....), show all the error messages on the screen & wait for user to press <F1> key
4F	1.If password is needed, ask for password 2.Clear the Energy Star logo (Green BIOS only)
50	Write all the CMOS values currently in the BIOS stack are back into the CMOS
52	1.Initialize all ISA ROMs 2.Later PCI initializations(PCI BIOS only), assign IRQ to PCI devices, initialize all PCI ROMs 3.PnP inits (PnP BIOS), assign IO, Memory, IRQ & DMA to PnP ISA devices, initialize all PnP ISA ROMs 4.Program shadow RAM according to setup setting 5.Program parity according to setup setting 6.Power Management initialization. Enable/Disable global PM, APM interface initialization
53	1.If it is not a PnP BIOS, initialize serial & parallel ports 2.Initialize time value in BIOS data area by translate the RTC time value into a timer tick value
60	Setup virus protection (boot sector) functionality according to setup setting
61	1.Try to turn on level 2 cache (if L2 cache already turned on in post 3D, this part will be skipped) 2.Set the boot up speed according to setup setting 3.Last chance for chipset initialization 4.Last chance for Power Management initialization (Green BIOS only) 5.Show the system configuration table
62	1.Setup daylight saving according to setup values 2.Program NUM lock, typematic rate & speed according to setup setting
63	1.If any change in hardware configuration, update ESCD infor (PnP BIOS only) 2.Clear memory used 3.Boot system via INT 19h
88	CPU failed to initialise-
FF	Boot

Version 6.0 (Jan 29, 1999)

Code	Name	Description
C0	Turn Off Chipset and CPU test	OEM Specific-Cache control
		Processor Status (1FLAGS) Verification. Tests the following processor status flags: Carry, zero, sign, overflow. The BIOS sets each flag, verifies They are set, then turns each flag off and verifies it is off. Read/Write/Verify all CPU registers except SS, SP, and BP with data pattern FF and 00. RAM must be periodically refreshed to keep the memory from decaying. This function ensures that the memory refresh function is working properly.
C1	Memory Presence	First block memory detect OEM Specific-Test to size on-board memory. Early chip set initialization Memory presence test OEM chip set routines Clear low 64K of memory Test first 64K memory.
C2	Early Memory Init	OEM Specific- Board Initialization
C3	Extend MemoryDRAM Select	OEM Specific- Turn on extended memory Initialization. Cyrix CPU initialization. Cache initialization.
C4	Special Display Handling	OEM Specific- Display/Video Switch Handling so that Switch Handling display switch errors never occurs
C5	Early Shadow	OEM Specific- Display/Video Switch Handling Handling so Switch Handling display switch errors never occur

Code	Name	Description
C6	Cache presence test	External cache size detection
CF	CMOS Check	CMOS checkup
B0	Spurious	If interrupt occurs in protected mode.
B1	Unclaimed NMI	If unmasked NMI occurs, display Press F1 to disable NMI, F2 reboot.
BF	Program Chip Set	To program chipset from default values
E1-EF	Setup Pages	E1- Page 1, E2 - Page 2, etc.
1	Force load Default to chipset	Chipset defaults program
2	Reserved	
3	Early Superio Init	Early Initialized the super IO
4	Reserved	
5	Blank Video	Reset Video controller
6	Reserved	
7	Init KBC	Keyboard controller init
8	KB test	Test the keyboard
9	Reserved	
A	Mouse Init	Initialized the mouse
B	Onboard Audio init	Onboard audio controller initialize if exist
C	Reserved	
D	Reserved	
E	CheckSum Check	Check the intergrity of the ROM,BIOS and message
F	Reserved	
10	Auto detec EEPROM	Check Flash type and copy write/erase routines to 0F000h segments
11	Reserved	
12	Cmos Check	Check CMOS Circuitry and reset
13	Reserved	
14	Chipset Default load	Program the chipset registers with CMOS Values
15	Reserved	
16	Clock Init	Init onboard clock generator
17	Reserved	
18	Identify the CPU	Check the CPU ID and init L1/L2 cache
19	Reserved	
1A	Reserved	
1B	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and Initialize INT 00h-1Fh according to INT_TBL
1C	Reserved	
1D	Early PM Init	First step initialize if single CPU Onboard
1E	Reserved	
1F	Re-initial KB	Re-init KB
20	Reserved	
21	HPM init	If support HPM, HPM get initialized here
22	Reserved	
23	Test CMOSInterface and battery status	Verifies CMOS is working correctly, and detects bad battery. If failed,load CMOS defaults and load into chipset
24	Reserved	
25	Reserved	
26	Reserved	
27	KBC final Init	Final Initial KBC and setup BIOS data area
28	Reserved	
29	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.

Code	Name	Description
2A	Reserved	
2B	Reserved	
2C	Reserved	
2D	Video memory test	Test video memory, write sign-on message. Setup shadow RAM - Enable shadow according to Setup.
2E	Reserved	
2F	Reserved	
30	Reserved	
31	Reserved	
32	Reserved	
33	PS2 Mouse setup	Setup PS2 Mouse and reset KB
34	Reserved	
35	Test DMA Controller 0	Test DMA channel 0
36	Reserved	
37	Test DMA Controller 1	Test DMA channel 1
38	Reserved	
39	Test DMA Page Registers	Test DMA Page Registers.
3A	Reserved	
3B	Reserved	
3C	Test Timer Counter 2	Test 8254 Timer 0 Counter 2.
3D	Reserved	
3E	Test 8259-1 Mask Bits	Verify 8259 Channel 1 masked interrupts by alternately turning off and on the interrupt lines.
3F	Reserved	
40	Test 8259-2 Mask Bits	Verify 8259 Channel 2 masked interrupts by alternately turning off and on the interrupt lines.
41	Reserved	
42	Reserved	
43	Test Stuck 8259's Interrupt Bits. Test 8259 Interrupt Functionality	Turn off interrupts then verify no interrupt mask register is on. Force an interrupt and verify the interrupt occurred.
44	Reserved	
45	Reserved	
46	Reserved	
47	Set EISA Mode	If EISA non-volatile memory checksum is good, execute EISA initialization. If not, execute ISA tests an clear EISA mode flag.
48	Reserved	
49	Size Base and Ext Memory	Size base memory from 256-640K and extended mem above 1MB.
4A	Reserved	
4B	Reserved	
4C	Reserved	
4D	Reserved	
4E	Size Base and Extended Memory	Size base memory from 256K to 640K and extended memory above 1MB using various patterns (this test is skipped in EISA mode and can be skipped with ESC key in ISA mode).
4F	Reserved	
50	USB init	Initialize USB controller
51	Reserved	
52	Memory Test	Test all memory of memory above 1MB using Virtual 8086 mode, page mode and clear the memory
53	Reserved	

Code	Name	Description
54	Reserved	
55	CPU display	Detect CPU speed and display CPU vendor specific version string and turn on all necessary CPU features
56	Reserved	
57	PnP Init	Display PnP logo and PnP early init
58	Reserved	
59	Setup Virus protect	Setup virus protect according to Setup
5A	Reserved	
5B	Awdflash Load	If required, will auto load Awdflash.exe in POST
5C	Reserved	
5D	Onboard I/O Init	Initializing onboard superIO
5E	Reserved	
5F	Reserved	
60	Setup enable	Display setup message and enable setup Functions
61	Reserved	
62	Reserved	
63	Initialize & install mouse	Detect if mouse is present, initialize mouse, install interrupt vectors.
64	Reserved	
65	PS2 Mouse special	Special treatment to PS2 Mouse port
66	Reserved	
67	ACPI init	ACPI sub-system initializing
68	Reserved	
69	Setup Cache controller	Initialize cache controller.
6A	Reserved	
6B	Setup Entering	Enter setup check and autoconfiguration check up
6C	Reserved	
6D	Initialise floppy drive & controller	Initialize floppy disk drive controller and any drives.
6E	Reserved	
6F	FDD install	Install FDD and setup BIOS data area parameters
70	Reserved	
71	Reserved	
72	Reserved	
73	Initialise hard drive & controller	Initialize hard disk drive controller and any drives.
74	Reserved	
75	Install HDD	IDE device detection and install
76	Reserved	
77	Detect & Initialize Serial/Parallel ports	Initialize any serial and parallel ports (also game port).
78	Reserved	
79	Reserved	
7A	Detect & Initialize Math Coprocessor	Initialize math coprocessor.
7B	Reserved	
7C	HDD Check for Write Protection	HDD check out
7D	Reserved	
7E	Reserved	
7F	POST error check	Check POST errors and display them and ask for user intervention
80	Reserved	
81	Reserved	

Code	Name	Description
82	Security Check	Ask password security (optional).
83	Write CMOS	Write all CMOS values back to RAM and clear screen.
84	Pre-boot Enable	Enable parity checker Enable NMI, Enable cache before boot.
85	Initialise Option ROMs	Initialize any option ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
86-92	Reserved	
93	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
94	Final Init	Final init for last micro details before boot
95	Special KBC patch	Set system speed for boot Setup NumLock status according to Setup
96	Boot Attempt	Set low stack Boot via INT 19h.
FF	Boot	

Version 6.0 (Jan 29, 1999) Quick Post

Code	Name	Description
65	Init onboard device	Early Initialized the super IO. Reset Video controller Keyboard controller init. Test the Keyboard Initialized the mouse. Onboard audio controller initialize if exist. Check intergraty of the ROM, BIOS and messageCheck Flash type and copy flash write/erase routines to 0F000h segments Check Cmos Circuitry and reset CMOS Program the chipset registers with CMOS values. Init onboard clock generator
66	Early Sytem setup	Check the CPU ID and init L1/L2 cache. Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR and initialize INT 00h-1Fh according to INT_TBL First step initialize if single CPU onboard. Re-init KBIf support HPM, HPM get initialized here
67	KBC and CMOS Init	Verifies CMOS working, detect bad battery. If failed, load defaults and load into chipset Final Initial KBC and setup BIOS data area.
68	Video Init	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter. Test video memory, write sign-on message to screen. Setup shadow RAM - Enable shadow according to Setup.
69	8259 Init	Init 8259 channel 1 and mask IRQ 9
6A	Memory test	Quick Memory Test
6B	CPU Detect and IO init	Detect CPU speed and display CPU vendor specific version stringand turn on necessary CPU features. Display PnP logo and PnP early initSetup virus protect according to Setup. If required, auto load Awdflash.exe in POST Initializing onboard super IO
6C	Reserved	
6D	Reserved	
6E	Reserved	
6F	Reserved	
70	Setup Init	Display setup message and enable setup functions. Detect if mouse is present, initialize mouse, install interrupt vectors. Special treatment to PS2Mouse port ACPI sub-system initializing.
71	Setup Cache controller	Initialize cache controller.
72	Install FDD	Enter setup and auto-configuration check up. Initialize floppy controller and drives. Install FDD and setup BIOS data area
73	Install HDD	Initialize hard drive controller and any drives. IDE device detection and install. Initialize any serial and parallel ports (also game port).
74	Detect & Initialize MathCoprocessor	Initialize math coprocessor.
75	HDD Check for Write Protection	HDD check out
76	Reserved	

Code	Name	Description
77	Display POST error	Check POST error and display them and ask for user interventionAsk password security (optional).
78	CMOS & Option ROM Init	Write all CMOS values back to RAM and clear screen. Enable parity checker. Enable NMI, Enable cache before boot. Initialize ROMs present from C8000h to EFFFFh. NOTE: When FSCAN option is enabled, ROMs initialize from C8000h to F7FFFh.
79	Reserved	
7A	Reserved	
7B	Reserved	
7C	Reserved	
7D	Boot Medium detection	Read and store boot partition head and cylinders values in RAM
7E	Final Init	Final init for last micro details before boot
7F	Special KBC patch	Set system speed for boot. Setup NumLock status as per Setup
80	Boot Attempt	Set low stackBoot via INT 19h.
FF	Boot	

Version 6.0 S4 Codes

Code	Name	Description
5A	Early Chipset Init	Early Initialized the super IO. Reset Video controller. Keyboard controller init. Test the Keyboard. Initilized the mouse
5B	CMOS Check	Check CMOS Circuitry and reset CMOS
5C	Chipset default Prog	Program the chipset registers with CMOS values.Init onboard clock generator
5D	Identify the CPU	Check the CPU ID and init L1/L2 cache
5E	Setup Interrupt Vector Table	Initialize first 120 interrupt vectors with SPURIOUS_INT_HDLR andINT 00h-1Fh according to INT_TBL. First step initialize if single CPU Onboard. Re-init KB. If support HPM, HPM get initialized Here.
5F	Test CMOS Interface & battery status	Verifies CMOS is working correctly, and detects bad battery. If failed, load CMOS defaults and load into chipset.
60	KBC final Init	Final Initial KBC and setup BIOS data area
61	Initialize Video Interface	Read CMOS location 14h to find out type of video in use. Detect and Initialize Video Adapter.
62	Video Memory Test	Test video memory, write sign-on message to screen.Setup shadow RAM - Enable shadow according to Setup.
63	Setup PS2 mouse and test DMA	Setup PS2 Mouse and reset KBTest DMA channel 0
64	Test 8259	Test 8259 channel 1 and mask IRQ 9
65	Init Boot Device	Detect if mouse is present, initialize mouse, install interrupt vectors.Special treatment to PS2 Mouse port ACPI sub-system initializingInitialize cache controller.
66	Install Boot Devices	Enter setup check and autoconfiguration check up. Initialize floppy disk drive controller and any drives. Install FDD and setup BIOS data area Parameters. Initialize hard drive controller and any drives. IDE device detection and install
67	Cache Init	Cache init and USB init
68	PM init	PM initialization
69	PM final Init and issue SMI	Final init Before resume
FF	Full on	

Version 6.0 Boot Block Codes

Code	Name	Description
1	Base memory test	Clear base memory area (0000:0000--9000:ffffh)
5	KB init	Initialized KBC
12	Install interrupt vectors	Install int. vector (0-77), and initialized 00-1fh to their proper place
0D	Init Video	Video initializing
41	Init FDD	Scan floppy and media capacity for onboard super IO
FF	Boot	Load boot sector

Award 6.0 Rev 1.0 11/03/99 Medallion (i810)

BOOT BLOCK CODES

Code	Meaning
CF	Test CMOS R/W functionality
C0	Early chipset initialization
C1	Detect memory
0C	BIOS checksum verify
C5	OEM Specific-Early Shadow enable for fast boot. Copy BIOS from ROM into shadow.
01	Clear base memory 0-640 Kb
05	Enable Keyboard Interface
0C	Initial interrupt vector 00-1Fh
0D	Detect and Initialize Video Adapter. If no display device, speaker will beep
41	Initialize floppy disk drive controller and detect media type
FF	SystemBooting

Code	Description
CFh	Test CMOS R/W functionality.
C0h	Early chipset init: Disable shadow RAM, L2 (socket 7 or below), Program basic chipset register
C1h	Detect memory, autodetect DRAM size, type, ECC. Autodetect L2 cache (socket 7 or below)
C3h	Expand compressed BIOS code to DRAM
C5h	Call chipset hook to copy BIOS back to E000 & F000 shadow RAM.
0h1	Expand the Xgroup codes locating in physical address 1000:0
03h	Initial Superio_Early_Init switch.
05h	1. Blank out screen 2. Clear CMOS error flag
07h	1. Clear 8042 interface 2. Initialize 8042 self-test
08h	Test special keyboard controller for Winbond 977 Super I/O chips. Enable keyboard interface.
0Ah	Disable PS/2 mouse interface (optional). Auto detect ports for keyboard & mouse followed by a port & interface swap (optional). Reset keyboard for Winbond 977 series Super I/O chips.
0Eh	Test F000h segment shadow to see whether R/W-able. If test fails, keep beeping speaker.
10h	Auto detect flash type to load appropriate flash R/W codes into the run time area in F000 for ESCD & DMI support.
12h	Use walking 1s to check interface in CMOS circuitry. Set RTC power status, check override.
14h	Program chipset default values into chipset. Default values are MODBINable by OEMs.
16h	Initial onboard clock generator if Early_Init_Onboard_Generator defined. See also 26h.
18h	Detect CPU information including brand, SMI type (Cyrix or Intel) and CPU level (586 or 686).
1Bh	Initial interrupts vector table. If no special specified, all H/W interrupts are directed to SPURIOUS_INT_HDLR & S/W interrupts to SPURIOUS_soft_HDLR.

Code	Description
1Dh	Initial EARLY_PM_INIT switch.
1Fh	Load keyboard matrix (notebook platform)
21h	HPM initialization (notebook platform)
23h	Check validity of RTC value- e.g. 5Ah is an invalid value for RTC minute. Load CMOS settings into BIOS stack. If CMOS checksum fails, use default value.
24h	Prepare BIOS resource map for PCI & PnP use. If ESCD is valid, take into consideration of the ESCD's legacy information.
25h	Early PCI Initialization: Enumerate PCI bus number. Assign memory & I/O resource. Search for a valid VGA device & VGA BIOS, and put it into C000:0
26h	If Early_Init_Onboard_Generator not defined Onboard clock generator init. Disable respective clock resource to empty PCI & DIMM slots. Init onboard PWM and H/W monitor devices
27h	Initialize INT 09 buffer
29h	Program CPU internal MTRR (P6 & PII) for 0-640K memory address. Initialize the APIC for Pentium class CPU. Program early chipset according to CMOS setup. Example: onboard IDE controller. Measure CPU speed.
2Bh	Invoke Video BIOS
2Dh	Initialize double-byte language font (Optional) Put information on screen display, including Award title, CPU type, CPU speed, full screen logo.
33h	Reset keyboard if Early_Reset_KB is defined e.g. Winbond 977 Super I/O chips. See 63h.
35h	Test DMA Channel 0
37h	Test DMA Channel 1.
39h	Test DMA page registers.
3Ch	Test 8254
3Eh	Test 8259 interrupt mask bits for channel 1.
40h	Test 8259 interrupt mask bits for channel 2.
43h	Test 8259 functionality.
47h	Initialize EISA slot
49h	Calculate total memory by testing the last double word of each 64K page.Program write allocation for AMD K5 CPU.
4Eh	Program MTRR of M1 CPU. Initialize L2 cache for P6 class CPU & program CPU with proper cacheable range.Initialize the APIC for P6 class CPU. On MP platform, adjust the cacheable range to smaller one in case the cacheable ranges between each CPU are not identical.
50h	Initialize USB Keyboard & Mouse.
52h	Test all memory (clear all extended memory to 0)
53h	Clear password according to H/W jumper (Optional)
55h	Display number of processors (multi-processor platform)
57h	Display PnP logo. Early ISA PnP initialization -Assign CSN to every ISA PnP device.
59h	Initialize the combined Trend Anti-Virus code.
5Bh	(Optional Feature) Show message for entering AWDFLASH.EXE from FDD
5Dh	Initialize Init_Onboard_Super_IO. Initialize Init_Onbaard_AUDIO.
60h	OK to enter Setup utility; i.e. not until this POST stage can users enter the CMOS setup utility.
63h	Reset keyboard if Early_Reset_KB is not defined.
65h	Initialize PS/2 Mouse
67h	Prepare memory size information for function call: INT 15h ax=E820h
69h	Turn on L2 cache
6Bh	Program chipset registers according to items described in Setup & Auto-configuration table.
6Dh	Assign resources to all ISA PnP devices. Auto assign ports to onboard COM ports if the corresponding item in Setup is set to "AUTO".
6Fh	Initialize floppy controller. Set up floppy related fields in 40:hardware.
75h	Detect & install all IDE devices: HDD, LS120, ZIP, CDROM…..
76h	(Optional) Enter AWDFLASH.EXE if found in floppy drive & ALT+F2 is pressed.

Code	Description
77h	Detect serial ports & parallel ports.
7Ah	Detect & install co-processor
7Ch	Init HDD write protect.
7Fh	Switch back to text mode if full screen logo is supported. If errors occur, report errors & wait for keys. If no errors occur or F1 key is pressed to continue: Clear EPA or customization logo.

E8POST.ASM STARTS

Code	Description
82h	Call chipset power management hook. Recover text fond used by EPA logo (not for full screen logo) If password is set, ask for password.
83h	Save all data in stack back to CMOS
84h	Initialize ISA PnP boot devices
85h	USB final Initialization. Switch screen back to text mode
87h	NET PC: Build SYSID Structure.
89h	Assign IRQs to PCI devices. Set up ACPI table at top of the memory.
8Bh	Invoke all ISA adapter ROMs. Invoke all PCI ROMs (except VGA)
8Dh	Enable/Disable Parity Check according to CMOS setup. APM Initialization
8Fh	Clear noise of IRQs
93h	Read HDD boot sector information for Trend Anti-Virus code
94h	Enable L2 cache. Program Daylight Saving. Program boot up speed. Chipset final initialization.Power management final initialization. Clear screen & display summary table. Program K6 write allocationProgram P6 class write combining
95h	Update keyboard LED & typematic rate
96h	Build MP table. Build & update ESCD. Set CMOS century to 20h or 19h. Load CMOS time into DOS timer tickBuild MSIRQ routing table.
FFh	Boot attempt (INT 19h)

Unexpected Errors

Code	Meaning
B0	If interrupt occurs in protected mode
B1	Unclaimed NMI occurs

v3.3

Code	Meaning	Code	Meaning
1-5	Keyboard controller	1F	Memory verifier
06	On board LSI	20-23	CPU support chips
07	CPU	24	Extended memory size
8-0E	CMOS; 8254; 8237; 8259; EPROM	25	Extended memory size
0F	Extended CMOS	26	Protected mode
10-14	Refresh	27-28	Shadow RAM
15	First 64K RAM	2A	Initialise keyboard
16	Interrupt vector tables	2B	Floppy drive initialisation
17	Video initialisation	2C	Serial port initialisation
18	Video memory	2D	Parallel port initialisation
19-1A	Interrupt line mask	2E	Hard disk initialisation

Code	Meaning	Code	Meaning
1B	Battery good	2F	Maths coprocessor
1C	CMOS checksum	30	Reserved
1D	CMOS chip	31	Optional ROMs
1E	Memory size	FF	Boot

CHIPS AND TECHNOLOGIES

Some displayed as decimal as well as to port 80 in hex. Micro Channel uses 680 and 3BC.

POST Procedures

Procedure	Meaning
Power On Tests	CPU synchronises with clock. Check the CPU or clock.
System ROM Check	The BIOS runs a checksum on itself. Check the BIOS chips.
DMA Controller Fail	DMA Controllers are initialised and tested. Check the DMA chips.
System Timer Failed	Channels 0/1/2 are tested in sequence. Check the PIT chips.
Base 64K Memory Testing	Walking-bit test on 1st 64K of RAM. Check for bad RAM chips or data or address line.
Interrupt Contr Failed	Test the 8259 chip.
CPU Still In Prot Mode	Attempts made to read configuration of system through 8042 keyboard controller.
Refresh Not Occurring	Memory refresh is tested; standard refresh is 120-140 ns. Check the PIT chip.
Keyboard Controller Not Responding	Tests are run on the keyboard controller. Check the 8042 chip.
Could Not Enter Protected Mode	BIOS attempts to enter protected mode to test extended memory. Check 8042 or A20.
Initialise Timer	Attempts are made to initialise the PIT.
Init DMA Controller	Attempts are made to initialise the DMA Controller.
Entering/Exiting Protected Mode	The transition is handled by the keyboard controller and the A20 line. Check the 8042 or the A20.
Relocate Shadow RAM	BIOS attempts to shadow itself into extended memory. Check for memory problems.
Test For EMS	Check the EMS adapter or an improper CMOS/Jumper setting.
Test Video Capabilities	Normally includes a memory test on the adapter memory up to 256K.
Test Memory	Extensive testing of Base, Extended, Expanded memory. Check for defective memory modules; 8042 chip; A20 line or an improper CMOS/Jumper setting.
Check System Options	The hardware in the system is compared with the values stored in CMOS. The PIT/PIC/8042/RTC and other system board chips are tested again.
Peripheral Check/Test	Checks made for peripherals at standard I/O ports including serial and parallel ports keyboards and coprocessors. Should see an error message on screen at this point.
Floppy Test	Floppy devices set in CMOS are checked and initialised. If a bootable floppy is found the fixed disks are tested and BIOS will boot to floppy. Check for defective controllers or an improper CMOS Setup.
Fixed Disk Test	Checks for fixed disks in CMOS. If no bootable floppy in A: drive, BIOS loads first sector off the first fixed disk and jumps to memory where the sector was loaded. You may just see a flashing cursor or an error message from the potential operating system. Check for improper CMOS setup/defective controller/fixed disk or corruption of bootloader software on the fixed disk.
Advanced Options	include mouse/cache etc. You should see an error message on the screen at this point, except that a defective cache may hang the system; in most cases, the cache will be disabled by the BIOS.

POST Codes

NEAT, PEAK/DM, OC8291, ELEAT BIOS

Hex	Dec	Code
00	00	Error in POS register.
01	01	Flag register failed.
02	02	CPU register failed.
03	03	System ROM did not checksum
04	04	DMA controller failed
05	05	System timer failed
06	06	Base 64K RAM failed address test,: not installed, misconfigured, bad addressing
07	07	Base 64K RAM failed data test
08	08	Interrupt controller failed
09	09	Hot (unexpected) interrupt occurred
0A	10	System timer does not interrupt
0B	11	CPU still in protected mode
0C	12	DMA page registers failed
0D	13	Refresh not occurring
0E	14	Keyboard controller not responding
0F	15	Could not enter protected mode
10	16	GDT or IDT failed
11	17	LDT register failed
12	18	Task register failed
13	19	LSL instruction failed
14	20	LAR instruction failed
15	21	VERR/VERW failed
16	22	Keyboard controller gate A20 failed
17	23	Exception failed/unexpected exception
18	24	Shutdown during memory test
19	25	Last used error code
1A	26	Copyright checksum error
1B	27	Shutdown during memory sizing
1C	28	CHIPSet initialization
50	80	Initialize hardware
51	81	Initialize timer
52	82	Initialize DMA controller
53	83	Initialize interrupt controller
54	84	Initialize CHIPSet
55	85	Setup EMS configuration
56	86	Entering protected mode for first time
57	87	Size memory chips
58	88	Configure memory chip interleave
59	89	Exiting protected mode for first time
5A	90	Determine system board memory size
5B	91	Relocate shadow RAM
5C	92	Configure EMS
5D	93	Set up wait state configuration
5E	94	Re-test 64K RAM
5F	95	Test shadow RAM

Hex	Dec	Code
60	96	Test CMOS RAM
61	97	Test video
62	98	Test and initialize DDNIL bits
63	99	Test protected mode interrupt
64	100	Test address line A20
65	101	Test memory address lines
66	102	Test memory
67	103	Test extended memory
68	104	Test timer interrupt
69	105	Test real time clock (RTC)
6A	106	Test keyboard
6B	107	Test 80x87 math chip
6C	108	Test RS232 serial ports
6D	109	Test parallel ports
6E	110	Test dual card
6F	111	Test floppy drive controller
70	112	Test hard drive controller
71	113	Test keylock
72	114	Test pointing device
90	144	Setup RAM
91	145	Calculate CPU speed
92	146	Check configuration
93	147	Initialize BIOS
94	148	POST Bootstrap
95	149	Reset ICs
96	150	PEAK: System board POS. NEAT/OC8291 ELEAT: Test/init cache and controller.
97	151	VGA Power on Diagnostics and setup
98	152	Adapter POS
99	153	Re-initialize DDNIL bits
A0	160	Exception 0
A1	161	Exception 1
A2	162	Exception 2
A3	163	Exception 3
A4	164	Exception 4
A5	165	Exception 5
A6	166	Exception 6
A7	167	Exception 7
A8	168	Exception 8
A9	169	Exception 9
AA	170	Exception A
AB	171	Exception B
AC	172	Exception C
AD	173	Exception D
C0	224	System board memory failure
C1	225	I/O Channel Check activated
C2	226	Watchdog timer timeout
C3	227	Bus timer timeout

COMPAQ

Port 84 codes show errors - 85 shows the category:

```
00      System BIOS
01      Error after boot
05      Video POST
```

General

Code	Meaning	Code	Meaning
00	Initialise flags	09	Reset code in CMOS byte
01	Read manufacturing jumper	0A	Vector Via 40:67 reset function
02	8042 Received Read command	0B	Vector Via 40:67 with E01 function
03	No response from 8042	0C	Boot reset function
04	Look for ROM at E000	0D	Test #2 8254 Counter 0
05	Look for ROM at C800	0E	Test #2 8254 Counter 2
06	Normal CMOS reset code	0F	Warm Boot
08	Initialise 8259		

Overall Power Up Sequence

Code	Meaning	Code	Meaning
10	PPI disabled	20	Test real and extended memory
11	Initialise (blast) VDU controller	21	Initialise time-of-day
12	Clear Screen; turn on video	22	Initialise 287 coprocessor
13	Test time 0	23	Test the keyboard and 8042
14	Disable RTC interrupts	24	Reset A20
15	Check battery power	25	Test diskette subsystem
16	Battery has lost power	26	Test fixed disk subsystem
17	Clear CMOS diags	27	Initialise parallel printer
18	Test base memory (first 128K)	28	Perform search for optional ROMs
19	Initialise base memory	29	Test valid system configuration
1A	Initialise VDU adapters	2A	Clear screen
1B	The system ROM	2B	Check for invalid time and date
1C	CMOS checksum	2C	Optional ROM search
1D	DMA controller/page registers	2D	Test timer 2
1E	Test keyboard controller	2F	Write to diagnostic byte
1F	Test 286 protected mode		

Base RAM Initialisation

Code	Meaning	Code	Meaning
30	Clear first 128K bytes of RAM	36	Check battery power
31	Load interrupt vectors 70-77	37	Check for game adapters
32	Load interrupt vectors 00-1F	38	Check for serial ports
33	Initialise MEMSIZE and RESETWD	39	Check for parallel printer ports
34	Verify CMOS checksum	3A	Initialise port and comm timeouts
35	CMOS checksum not valid	3B	Flush keyboard buffer

Base RAM Test

Code	Meaning	Code	Meaning
40	Save RESETWD value	44	Start verify of 128K RAM test
41	Check RAM refresh	45	Check for parity errors
42	Start write of 128K RAM test	46	No RAM errors
43	Rest parity checks	47	RAM error detected

VDU Initialisation and Test

Code	Meaning	Code	Meaning
50	Check for dual frequency in CMOS	58	Start of VDU test (each adapter)
51	Check CMOS VDU configuration	59	Check existence of adapter
52	Start VDU ROM search	5A	Check VDU registers
53	Vector to VDU option ROMs	5B	Start screen memory test
54	Initialise first display adapter	5C	End test of adapter
55	Initialise second display adapter	5D	Error detected on an adapter
56	No display adapters installed	5E	Test the next adapter
57	Initialise primary VDU mode	5F	All adapters successfully tested

Memory Test

Code	Meaning	Code	Meaning
60	Start of memory tests	6B	Display error message
61	Enter protected mode	6C	End of memory test
62	Start memory sizing	6D	Initialise KB OK string
63	Get CMOS size	6E	Determine size to test
64	Start test of real memory	6F	Start MEMTEST
65	Start test of extended memory	70	Display XXXXXKB OK
66	Save size memory (base	71	Test each RAM segment
67	128K option installed CMOS bit	72	High order address test
68	Prepare to return to Real Mode	73	Exit MEMTEST
69	Back in Real Mode-successful	74	Parity error on bus
6A	Protected mode error during test		

80286 Protected Mode

Code	Meaning	Code	Meaning
75	Start protected mode test	7B	Exit protected test
76	Prepare to enter protected mode	7C	High order address test failure
77	Test software exceptions	7D	Entered cache controller test
78	Prepare to return to Real Mode	7E	Programming memory cache
79	Back in Real Mode-successful	7F	Copy system ROM to high RAM
7A	Back in Real Mode-error occurred		

8042 and Keyboard

Code	Meaning	Code	Meaning
80	Start of 8042 test	88	Got result
81	Do 8042 self test	89	Test for stuck keys
82	Check result received	8A	Key seems to be stuck
83	Error result	8B	Test keyboard interface
84	OK 8042	8C	Got result
86	Start test	8D	End of Test
87	Got acknowledge		

System Board Test

Code	Meaning	Code	Meaning
90	Start of CMOS test	94	Page registers seem OK
92	CMOS seems to be OK	95	DMA controller is OK
92	Error on CMOS read/write test	96	8237 initialisation is complete
93	Start of DMA controller test	97	Start of NCA RAM test

Diskette Test

Code	Meaning	Code	Meaning
A0	Start of diskette tests	B2	Combo controller failed-exit
A1	FDC reset active (3F2h bit 2)	B3	Testing drive 1
A2	FDC reset inactive (3F2h bit 2)	B4	Testing drive 2
A3	FDC motor on	B5	Drive error (error condition)
A4	FDC timeout error	B6	Drive failed (failed to respond)
A5	FDC failed reset	B7	No fixed drives-exit
A6	FDC passed reset	B8	Fixed drive tests complete
A8	Start to determine drive type	B9	Attempt to boot diskette
A9	Seek operation initiated	BA	Attempt to boot fixed drive
AA	Waiting for FDC seek status	BB	Boot attempt failed FD/HD
AF	Diskette tests completed	BC	Boot record read, jump to boot record
B0	Start of fixed disk drive tests	BD	Drive error, retry booting
B1	Combo board not found-exit	BE	Weitek coprocessor test

EISA TESTS (Deskpro/M, /LT, /33L, P486c)

Code	Meaning	Code	Meaning
C0	EISA non-volatile memory checksum	C5	EISA display config error messages
C1	EISA DDF map initialization	C6	EISA PZ initialization begun
C2	EISA IRQ initialization	C7	EISA PZ initialization done
C3	EISA DMA initialization	C8	System manager board self-test
C4	EISA slot initialization		

LT, SLT, LTE

Code	Meaning	Code	Meaning
C0	Disable NMI	C6	Update BIOS time of day
C1	Turn off hard disk subsystem	C7	Turn on hard disk/modem subsystems
C2	Turn off video subsystem	C8	Turn on floppy disk subsystem
C3	Turn off floppy disk subsystem	C9	Turn on video subsystem
C4	Turn off hard disk/modem subsystems	CB	Flush keyboard input buffer
C5	Go to standby	CC	Re-enable MNI

Standard POST Functions

Code	Meanings	Code	Meaning
D0	Entry to clear memory routine	D5	Clr base mem, CLIM reg init fail SLT/286
D1	Ready to go to protected mode	D7	Scan and clear DDNIL bits
D2	Ready to clear extended memory	D9	Orvonton 4-way cache detect
D3	Ready to reset back to real mode	DD	Built-in self-test failed
D4	Back in real mode, ready to clear		

Option ROM Replacement

Code	Meaning	Code	Meaning
E0	Ready to replace E000 ROM	E9	Receiving for serial external boot sector
E1	Completed E000 ROM replacement	EA	Looking for parallel external boot ID str
E2	Ready to replace EGA ROM	EB	Receiving parallel external boot sector
E3	Completed EGA ROM replacement	EC	Boot record read, jump to boot record
E8	Looking for serial external boot ID str		

Port 85=05 (Video POST)

Code	Meaning	Code	Meaning
00	Entry into video option ROM	50	Slot type conflict error
01	Alternate adapter tests	51	Video memory conflict error
02	Vertical sync tests	52	ROM conflict error
03	Horizontal sync tests	60	Red DAC stuck low error
04	Static tests	61	Green DAC stuck low error
05	Bus tests	62	Blue DAC stuck low error
06	Configuration tests	63	DAC stuck high error
07	Alternate ROM tests	64	Red DAC fault error
08	Colour gun off tests	65	Green DAC fault error
09	Colour gun on tests	66	Blue DAC fault error
0A	Video memory tests	70	Bad alternate ROM version
0B	Board present tests	80	Colour gun stuck ON base code
10	Illegal configuration error	90	Colour gun stuck OFF base code
20	No vertical sync present	A0	Video memory failure base code
21	Vertical sync out of range	F0	Equipment failure base code
30	No horizontal sync present	00	Video POST over (also send 00 to 85)
40	Colour register failure		

After POST, the OS is booted. If a run-time error is detected, code 01 is sent to port 85, and the error code to port 84 before booting. Here are run-time codes:

Code	Meaning	Code	Meaning
10	Entered dummy end-of-interrupt routine	14	Illegal opcode instruction encountered
11	Entered int 2 module (parity error)	15	Entered dum iret module
12	Emulating lock instruction	16	Entered irg9 module
13	Emulating loadall instruction	17	Entered 287err module

286 DeskPro

Code	Meaning	Code	Meaning
01	CPU	42	Printer Date
02	Coprocessor	43	Printer Pattern Test
03	DMA	48	Printer Failed
04	Interrupt Controller	51	VDU Controller Test
05	Port 61	52	VDU Controller Test
06	Keyboard Controller	53	VDU Attribute Test
07	CMOS	54	VDU Character Set Test
08	CMOS	55	VDU 80x25 Mode
09	CMOS	56	VDU 80x25 Mode
10	Programmable Timer	57	VDU 40x25 Mode
11	Refresh Detect Test	60	Diskette Drive ID Test
12	Speed Test	61	Format
14	Speaker Test	62	Read Test
21	Memory Read/Write	63	Write/Read Compare Test
24	Memory Address	64	Random Seek
25	Walking I/O	65	ID Media Test
31	Keyboard Short Test	66	Speed Test
32	Keyboard Long Test	67	Wrap Test
33	Keyboard LED Test	68	Write Protect Test
35	Security Lock Test	69	Reset Controller Test
41	Printer Failed		

386 DeskPro

Code	Meaning	Code	Meaning
01	I/O ROM Error	41	Printer Error
02	System Memory Board Failure	42	Mono Adapter Failure
12	System Option Error	51	Display Adapter Failure
13	Time and Date not set	61	Diskette Controller Error
14	Memory Size Error	62	Diskette Boot Recorder Error
21	Memory Error	65	Diskette Drive Error
23	Memory Address Error	67	Ext FDC Failed-Go To Internal F
25	Memory Error	6A	Floppy Port Address Conflict
26	Keyboard Error	6B	Floppy Port Address Conflict
33	Keyboard Controller Error	72	Coprocessor Detection
34	Keyboard or System Unit Error		

486 DeskPro

Code	Meaning	Code	Meaning
01	CPU Test Failed	34	Keyboard Typematic Test Failed
02	Coprocessor or Weitek Error	41	Printer Failed or Not Connected
03	DMA Page Registers	42	Printer Data Register Failed
04	Interrupt Controller Master	43	Printer Pattern Test
05	Port 61 Error	48	Printer Not Connected
06	Keyboard Controller Self Test	51	Video Controller Test Failed
07	CMOS RAM Test Failed	52	Video Memory Test Failed
08	CMOS Interrupt Test Failed	53	Video Attribute Test Failed
09	CMOS Clock Load Data Test	54	Video Character Set Test Failed
10	Programmable Timer	55	Video 80x25 Mode
11	Refresh Detect Test Failed	56	Video 80x25 Mode
12	Speed Test Slow Mode out of range	57	Video 40x25 Mode Test Failed
13	Protected Mode Test Failed	58	Video 320x200 Mode Colour Set 1
14	Speaker Test Failed	59	Video 320x200 Mode Colour Set 1
16	Cache Memory Configuration	60	Diskette ID Drive Types Test
19	Installed Devices Test	61	Diskette Format Failed
21	Memory Machine ID Test Failed	62	Diskette Read Test Failed
22	Memory System ROM Checksum	63	Diskette Write
23	Memory Write/Read Test Failed	65	Diskette ID Media Failed
24	Memory Address Test Failed	66	Diskette Speed Test Failed
25	Walking I/O Test Failed	67	Diskette Wrap Test Failed
26	Increment Pattern Test Failed	68	Diskette Write Protect Test
31	Keyboard Short Test, 8042	69	Diskette Reset Controller Test
32	Keyboard Long Test Failed	82	Video Memory Test Failed
33	Keyboard LED Test, 8042	84	Video Adapter Test Failed

DELL

OEM version of Phoenix, Port 80. Also uses Smartvu display on front.

Code	Beeps	SmartVu	Meaning
01	1-1-2	Regs xREG xCPU(2)	CPU register test in progress
02	1-1-3	CMOS xCMS	CMOS write/read test failed
03	1-1-4	BIOS xROM	ROM BIOS checksum bad
04	1-2-1	Timr xTMR	Programmable interval timer failed
05	1-2-2	DMA xDMA	DMA initialization failed
06	1-2-3	Dpge xDPG	DMA page register write/read bad
08	1-3-1	Rfsh xRFH	RAM refresh verification failed
09	1-3-2	Ramp RAM?	First 64K RAM test in progress
0A	1-3-3	xRAM	First 64K RAM chip or data line bad, multi-bit
0B	1-3-4	xRAM	First 64K RAM odd/even logic bad
0C	1-4-1	xRAM	Address line bad first 64K RAM
0D	1-4-2	64K? x64K	Parity error detected in first 64K RAM
10	2-1-1		Bit 0 first 64K RAM bad
11	2-1-2		Bit 1 first 64K RAM bad

Code	Beeps	SmartVu	Meaning
12	2-1-3		Bit 2 first 64K RAM bad
13	2-1-4		Bit 3 first 64K RAM bad
14	2-2-1		Bit 4 first 64K RAM bad
15	2-2-2		Bit 5 first 64K RAM bad
16	2-2-3		Bit 6 first 64K RAM bad
17	2-2-4		Bit 7 first 64K RAM bad
18	2-3-1		Bit 8 first 64K RAM bad
19	2-3-2		Bit 9 first 64K RAM bad
1A	2-3-3		Bit 10 first 64K RAM bad
1B	2-3-4		Bit 11 first 64K RAM bad
1C	2-4-I		Bit 12 first 64K RAM bad
1D	2-4-2		Bit 13 first 64K RAM bad
1E	2-4-3		Bit 14 first 64K RAM bad
1F	2-4-4		Bit 15 first 64K RAM bad
20	3-1-1	SDMA xDMS	Slave DMA register bad
21	3-1-2	MDMA xDMM	Master DMA register bad
22	3-1-3	PICO xICO	Master interrupt mask register bad
23	3-1-4	PIC1 xIC1	Slave interrupt mask register bad
25	3-2-2	Intv	Interrupt vector loading in progress
27	3-2-4	Kybd xKYB	Keyboard controller test failed
28	3-3-1	CmCk	CMOS power bad; calculating checksum
29	3-3-2	Cnfg	CMOS configuration validation in progress
2B	3-3-4		Video memory test failed
2C	3-4-1	CRTI	Video initialization failed
2D	3-4-2		Video retrace failure
2E	3-4-3	CRT?	Search for video ROM in progress
30	none		Screen operable, running with video ROM
31	none		Monochrome monitor operable
32	none		Colour monitor (40 column) operable
33	none		Colour monitor (80 column) operable

Non-Fatal Error Meanings tor ATs

Only if Manufacturing Jumper is on POST

Code	Beeps	Smartvu	Meaning
34	4-2-1	Tick	Timer tick interrupt test in progress or bad
35	4-2-2	Shut	Shutdown test in progress or bad
36	4-2-3	A20	Gate A20 bad
37	4-2-4		Unexpected interrupt in protected mode
38	4-3-1	Emem	RAM test in progress or high address line bad > FFFF
3A	4-3-3	Tmr2	Interval timer channel 2 test or bad
3B	4-3-4	Time	Time-of-Day clock test or bad
3C	4-4-1	Asyn	Serial port test or bad
3D	4-4-2	Prnt	Parallel port test or bad
3E	4-4-3		Math coprocessor test or bad
3F	4-4-4	XCsh	Cache test failure

DTK

Evolved from ERSO (Taiwan).

Post Procedures-Symphony 486 BIOS

Procedure	Meaning
Init Interrupt Controller	Check the PIC chips.
Initialise Video Card	
Initialise DMA Controller	
Initialise Page Register	Check the 74612 chips.
Test Keyboard Controller	Internal operations of the keyboard controller are tested (8042).
Initialise DMA Contr/Timer	DMA registers and CMOS status bytes 0E/0F cleared. BIOS initialises 8254. Check the DMS or PIT chips.
DRAM Refresh Testing	
Base 64K Memory Testing	Walking-bit test of 1st 64K RAM. Check bad chips or data or address line.
Set System Stack	Part of memory is set aside by BIOS as a stack. Check bad DMA/memory.
Read System Configuration via 8042	Check for incorrect setup or bad keyboard controller or CMOS chip.
Test Keyboard Clock and Data Line	Keyboard's handling of A20 tested, and internal clock. Check keyboard controller or a bad address line.
Determine Video Type	
Check RS232/Printer	Test serial/parallel ports. Check I/O cards.
FDC Check	Test floppy controller. Check the drive as well.
Count Shadow RAM	Run memory tests. Check for bad memory chips address lines or data lines.
Show Total Mem/Return Real Mode	Total memory displayed and return to real mode. Keyboard or A20.
Back to Real Mode	Transition attempted through A20 line and keyboard controller.
Check HDC	The hard drive controller is tested.
Check FDD	Attempts are made to initialise the floppy drives.
Turn off Gate A20 and Test CoPro	Ttransition back to real mode by disabling A20 then copro tested. Check keyboard controller coprocessor or improper setup.
Set Time and Date	Time and date will be read from the RTC.

POST Codes

Code	Meaning	Code	Meaning
01	Power on start	48	Video 80 x 25 mode initialisation
03	Initialise interrupt controller-8259	4D	Display DTK BIOS title
05	Initialise video card-MCA and CGA	4F	Check RS232 and printer
0D	Initialise DMA controller-8237	50	FDC check
0E	Initialise page register-74612	55	Count shadow RAM
12	Test keyboard controller-8042	58	Display total memory, return to real mode
16	Initialise DMA controller and timer	5A	Back to real mode
22	DRAM refresh testing	60	Check HDC
25	Base 64K memory testing	62	Check FDD
30	Set system stack	65	Check HDC
33	Read system configuration through 8042	67	Initialise FDC and HDC
37	Test keyboard clock and data line	6A	Turn off gate A20 and test coprocessor
40	Determine video type	70	Set time and date according to RTC
44	Testing MGA and CGA if existing	77	Boot

EUROSOFT

See Mylex/Eurosoft.

FARADAY A-TEASE

Owned by Western Digital.

Code	Meaning	Code	Meaning
01	CPU test failed	1E	Check CMOS real time clock
02	BIOS ROM checksum test	1F	Generate and verify CMOS RAM checksum
03	Shutdown	21	Initialize PROM drivers
04	DMA page register test	22	Test parallel port loopback
05	8254 timer test	23	Test serial port loopback
06	Start refresh	24	Test CMOS real time clock
07	8042 keyboard controller test	25	Test shutdown
08	Test lower 128K RAM	26	Test memory over 1mb; output codes for errors 80-FF
09	Setup video	80	Divide overflow
0A	Test 128K-640K	81	Single step
0B	Test DMA controller #1	82	NMI
0C	Test DMA controller #2	83	Breakpoint
0D	Test interrupt controller #1	84	Int 0 detect
0E	Test interrupt controller #2	85	Bound error
0F	Test control port	86	Invalid opcode
10	Test parity	87	Processor extension not available
11	Test CMOS RAM	88	Double exception
12	Test for manufacturing mode	89	Processor ext segment error
13	Set up interrupt vectors	8A	Invalid task state segment
14	Test keyboard	8B	Segment not present
15	Configure parallel port	8C	Stack segment not present
16	Configure serial ports	8D	General protection error
17	Configure lower 640K RAM	8E	General protection error
18	Configure RAM above 1 Mb	8F	General protection error
19	Configure keyboard	90	Processor extension error
1A	Configure floppy drive	91-FF	Spurious interrupts (except F3 and F0)
1B	Configure hard drive	F3	CPU virtual (protected mode) test error
1C	Configure game card	F0	Virtual block move error
1D	Configure 80287 math chip		

HEADSTART

See Philips.

HP

Derived from Phoenix, all POST information is sent to the screen.

Vectra

A failure during POST will emit four beeps, and a 4-digit hex code to the monitor. Failures that occur before EGA/VGA monitors are initialised will not be displayed, so use a mono instead. BIOSes prior to March 1989 initialised the video before getting on with the POST.

POST PROCEDURES

Code	Meaning
CPU	Registers in CPU tested with data patterns; error flags are set, verified and reset.
BIOS Checksum	Checksums are performed on High and low BIOS Chips.
PIC Test	Test Timer Channels 0-2 then the memory refresh signal. Initialise timer if tests are passed. Check the 8254 chip.
64K Test	Walking-bit and address collision tests are performed on the first 64K of memory. Check for a bad memory chip or address line.
Cache Controller	Test the CPU cache controller and memory.
Video Adapter	Initialise the video adapter. If EGA/VGA is present wait for adapter to finish internal diagnostics. check the adapter or for improper setup.
DMA Test	Bit-patterns written to all DMA controller registers (inc page registers) and verifies the patterns written. If tests pass, registers are reset and the controller initialised.
PIC Test	Test mask register of master and slave interrupt controllers. Generate interrupt and monitor CPU to test success. Failure is normally down to the PIC but the interrupt test uses the BIOS clock (interrupt) and the RTC so check those.
Keyboard Controller	Perform several tests on the 8042 keyboard controller then send a series of interrupt request commands via the 8259 PIC.
HP-HIL Test	Test HP-HIL (Hardware Interrupt Level) controller with data patterns and verify it.
CMOS Test	Perform a checksum on the standard and extended CMOS RAM areas; perform a register test and check Byte 0D to determine power status. Check the CMOS extended CMOS RAM or battery respectively.
Manufacturing Test	Search for diagnostic tool used in manufacturing and run predetermined tests if found. Otherwise continue POST.
Base Memory Test	Test RAM between 64-640K with several pattern tests; the bit failure and bank can be determined by the displayed hex code.
Ext Memory Test	Test extended memory found. Bank and failing bit displayed by the hex code.
RTC Test	Test the RTC portion of the CMOS chip.
Keybrd Contr	Test keyboard controller; initialise k/b if no errors.
Floppy Disk	Test and initialise floppy controllers and drives found; check specific errors with displayed hex code. Check for correct setup or defective CMOS chip or battery.
Maths Copro	Test NPU registers and interrupt request functions.
CPU Clock Test	Test interface between CPU and system at different speeds. Check for incorrect clock setting for system peripherals or a bad CPU or clock generator chip.
Serial/Parallel Test	Test and initialise serial/parallel ports. Failure here will not halt the POST. The Vectra RS BIOS does not test the parallel port.
Boot	Initialise the BIOS vector table; standard and extended CMOS data areas and any adapter ROMs present. Then call Int 19 and give control to the boot loader. Failures past this point are usually down to the hard drive or corrupt OS code.

POST CODES

Code	Meaning	Code	Meaning
01	LED test	18	RAM address line independence test
02	Processor test	19	Size extended memory
03	System (BIOS) ROM test	20	Real-Mode memory test (first 640K)
04	RAM refresh timer test	21	Shadow RAM test
05	Interrupt RAM test	22	Protect Mode RAM test (extended RAM)
06	Shadow System ROM BIOS	23	Real Time clock test
07	CMOS RAM test	24	Keyboard test
08	Internal cache memory test	25	Mouse test
09	Initialize the Video Card	26	Hard disk test
10	Test external cache	27	LAN test
11	Shadow option ROMs	28	Flexible disk controller subsystem test
12	Memory Subsystem test	29	Internal numeric coprocessor test
13	Initialize EISA/ISA hardware	30	Weitek coprocessor test
14	8042 self-test	31	Clock speed switching test
15	Timer 0/Timer 2 test	32	Serial Port test
16	DMA Subsystem test	33	Parallel Port test
17	Interrupt controller test		

Vectra ES

Code	Meaning	Code	Meaning
000F	80286 CPU is bad		X=9 Y>0=Bad U42 Z>0=Bad U32
0010	Bad checksum on ROM 0	5XYZ	Lower 640K failed marching ones test
0011	Bad checksum on ROM 1		X = bbbx = > bbb (0-7) is # of 128K bank
011X	One RTC register is bad; Register = x(0-D)		bbb0 = > Indicate even byte bad
0120	RTC failed to tick		bbb1 = > Indicate odd byte bad
0240	CMOS/RTC has lost power		YZ = bbbb bbbb = > Bits (b = 1 are bad)
0241	Invalid checksum, IBM CMOS area	61XY	RAM address line XY stuck
0280	Invalid checksum, HP CMOS area		Some address lines to RAM stuck to 0 or 1
02XY	A CMOS register is bad; Register = XY - 40		XY = 00bb bbbb = > address bbbbbb stuck
0301	8042 failed to accept the reset command		XY = 01bb bbbb = > Multiple address lines are stuck (bbbbbb is the first bad one)
0302	8042 failed to respond to reset command	620X	Lower 640K parity error; Bank X
0303	8042 failed to reset		X = Address in 64K bank with parity error
0311	8042 failed to accept "WRITE CMD BYTE"		if X = 0 to y, U21 and/or U31 is/are bad
0312	8042 failed to accept the data of above cmd		if X = 8 to 9, U11 and/ore U41 is/are bad
0321	8042 failed to accept scancode from port 68	63XY	Parity error above 1MB; Bank XY
0322	8042 failed to respond to above scancode		Parity error during RAM test above first MB
0323	8042 responded incorrectly to scancode		XY = Address in 64K bank with parity error
0331	8042 failed to accept command from port 6A	6400	Parity generator failed to detect error
0332	8042 failed to generate SVC on port 67	71XY	Master 8259 failed R/W; bits XY
0333	8042 generated HPINT type on port 65		XY = bbbb bbbb + > bits (b = 1 is bad)
0334	8042 failed the R/W register on port 69	72XY	Slave 8259 failed R/W; bits XY
0335	8042 failed to generate HPINT on IRQ 15		XY = bbbb bbbb = > bits (b = 1 is bad)
0336	8042 failed to generate HPINT on IRQ 12	7400	Master 8259 failed interrupt
0337	8042 failed to generate HPINT on IRQ 11	7500	Slave 8259 failed interrupt

Code	Meaning	Code	Meaning
0338	8042 failed to generate HPINT on IRQ 10	9XYZ	Floppy drive controller error
0339	8042 failed to generate HPINT on IRQ 7		X=drive #
033A	8042 failed to generate HPINT on IRQ 5		Y=0=1st level error
033B	8042 failed to generate HPINT on IRQ 4		Z=0 Unsuccessful input from FD
033C	8042 failed to generate HPINT on IRQ 3		Z=1 Unsuccessful output to FDC
0341	8042 failed keyboard interface test comd		Z=2 Error while executing seek
0342	8042didn't respond to interface command		Z=3 Error during recalibrate
0343	Keyboard clock line stuck low		Z=4 Error verifying RAM buffer
0344	Keyboard clock line stuck high		Z=5 Error while resetting FDC
0345	Keyboard data line stuck low		Z=6 Wrong drive identified
0346	Keyboard data line stuck high		Z=7 Wrong media identified
0350	No ACK from keyboard self test command		Z=8 No interrupt from FDC
0351	Bad ACK from keyboard self test command		Z=9 Failed to detect track 0
0352	Keyboard is dead or not connected		Z=A Failed to detect index pulse
0353	No result from keyboard self test command		Y>1=Higher level error
0354	Keyboard self test failed		Y=1=Read sector error, side 0
0401	8042 failed to enable gate A-20		Y=2=Read sector error, side 1
0503	Serial port dead or non existent		Y=3=Write sector error, side 0
0505	Serial port fails port register tests		Y=4=Write sector error, side 1
0543	Parallel port dead or non-existent		Y=5=Format sector error, side 0
06XX	Stuck key; XX=scancode of key		Y=6=Format sector error, side 1
0700	Failed to switch to slow mode		Y=7=Read ID error, side 0
0701	Failed to switch to dynamic mode		Y=8=Read ID error, side 1
0702	Timer (channel 0) failed to interrupt		Z=1=No ID address mark
0703	Memory cycles too slow in slow mode		Z=2=No data address mark
0704	Memory cycles too fast in slow mode		Z=3=Media is write protected
0705	I/O cycles too slow in slow mode		Z=4=Sector # wrong
0706	I/O cycles too fast in slow mode		Z=5=Cylinder # wrong
0707	Memory cycles too slow in dynamic mode		Z=6=Bad cylinder
0708	Memory cycles too fast in dynamic mode		Z=7=DMA overrun
0709	I/O cycles too slow in dynamic mode		Z=8=ID CRC error
070A	I/O cycles too fast in dynamic mode		Z=9=Data CRC error
110X	Timer channel failed to register test (X)		Z=A=End of cylinder
1200	Memory refresh signal stuck high		Z=B=Unrecognizable error
1201	Memory refresh signal stuck low	A001	No 80287 detected
211X	DMA 1 failed R/W test at register x (0-7)	A002	80287 failed stack register R/W test
212X	DMA 2 failed R/W test at register x (0-7)	A00C	No zero-divide interrupt from 80287
221X	Bad DMA page register; X=register 0-7	CXYZ	R/W error on extended RAM in XY bank
300X	HP-HIL controller failed self test; X=data		Read/Write test failure on extended RAM
	X = xx1 = >read/write fail with data = 0DA5h		X = 0 = > Even byte is bad
	X = xx1x = >R/W fail with data = 0DA5h		X = 1 = > Odd byte is bad
	X = x1xx = >R/W fail with data = 0DA5h		XY = 64K bank where RAM failed
	X = 1xxx = >R/W fail with data = 0DA5h	CFFF	Extended RAM marching ones failed
3010	HP-HIL device test failed		Marching on test failure on extended RAM
4XYZ	Lower 640K failed R/W test;		X = 0 = > Even byte bad
	X=0,2,4,6 Y>0=Bad U23 Z>0=Bad U13		X = 1 = > Odd byte bad
	X=1,3,5,7 Y>0=Bad U43 Z>0=Bad U33		XA = 64K bank where RAM failed
	X=8 Y>0=Bad U22 Z>0=Bad U12		

Vectra QS & RS

Code	Meaning	Code	Meaning
000F	386 CPU bad	620X	Lower 640K parity error; Bank X
0010	Bad checksum on ROM 0		X = Address in 64K bank where parity occurred
0011	Bad checksum on ROM 1	63XY	Parity error above 1MB; Bank XY
011X	RTC register is bad		XY = Address in 64K bank where parity occurred
0120	RTC failed to tick	6500	Shadow RAM bad at BIOS segment
0240	CMOS/RTC lost power	5XYZ	Lower 640K failed marching ones test
0241	Invalid checksum, IBM CMOS area		RAM in lower 640K failed read/write test
0280	Invalid checksum, HP CMOS area		X = bbcc = > bb is # 64K of 32 bit word bank
02XY	Bad CMOS register, at XY-40		cc = 00 = > byte 0 is bad
0301	8042 failed to accept reset command		cc = 01 = > byte 1 is bad
0302	8042 failed to respond to reset		cc = 02 = > byte 2 is bad
0303	8042 failed on reset		cc = 03 = > byte 3 is bad
0311	8042 didn't accept "WRITE CMD BYTE"		YZ = bbbb bbbb = > bits (b = 1 are bad)
0312	8042 didn't accept data		
0321	8042 failed to accept scancode, port 68	6510	Shadow RAM bad at HP EGA segment
0322	8042 failed to respond to scancode	71XY	Master 8259 failed R/W; bits XY
0323	8042 responded incorrectly to scancode		XY = bbbb bbbb = > bits which b = 1 is bad
0331	8042 failed to accept command from port 6A	72XY	Slave 8259 failed R/W; bits XY
0332	8042 failed to generate SVC on port 67		XY = bbbb bbbb = > bits which b = 1 is bad
0333	8042 generated HPINT type on port 65	7400	Master 8259 failed interrupt
0334	8042 failed the R/W register on port 69	7500	Slave 8259 failed interrupt
0335	8042 failed to generate HPINT on IRQ 15	9XYZ	Floppy drive controller error
0336	8042 failed to generate HPINT on IRQ 12		X=drive #
0337	8042 failed to generate HPINT on IRQ 11		Y=0=1st level error
0338	8042 failed to generate HPINT on IRQ 10		Z=0 Unsuccessful input from FD
0339	8042 failed to generate HPINT on IRQ 7		Z=1 Unsuccessful output to FDC
033A	8042 failed to generate HPINT on IRQ 5		Z=2 Error while executing seek
033B	8042 failed to generate HPINT on IRQ 4		Z=3 Error during recalibrate
033C	8042 failed to generate HPINT on IRQ 3		Z=4 Error verifying RAM buffer
0341	8042 failed interface test command		Z=5 Error while resetting FDC
0342	8042didn't respond to interface command		Z=6 Wrong drive identified
0343	Keyboard clock line stuck low		Z=7 Wrong media identified
0344	Keyboard clock line stuck high		Z=8 No interrupt from FDC
0345	Keyboard data line stuck low		Z=9 Failed to detect track 0
0346	Keyboard data line stuck high		Z=A Failed to detect index pulse
0350	No ACK from keyboard self test command		Y>1=Higher level error
0351	Bad ACK from keyboard self test command		Y=1=Read sector error, side 0
0352	Keyboard is dead or not connected		Y=2=Read sector error, side 1
0353	No result from keyboard self test command		Y=3=Write sector error, side 0
0354	Keyboard self test failed		Y=4=Write sector error, side 1
0401	8042 failed to enable gate A-20		Y=5=Format sector error, side 0
0503	Serial port dead or non-existent		Y=6=Format sector error, side 1
0505	Serial port fails port register tests		Y=7=Read ID error, side 0
06XX	Stuck key; XX=scancode of key		Y=8=Read ID error, side 1
0700	Failed to switch to slow speed		Z=1=No ID address mark

Code	Meaning	Code	Meaning
0701	Failed to switch to fast speed		Z=2=No data address mark
0702	Timer failed to interrupt		Z=3=Media is write protected
0703	CPU clock too slow in slow speed		Z=4=Sector # wrong
0704	CPU clock too fast in slow speed		Z=5=Cylinder # wrong
0707	CPU clock too slow in fast speed		Z=6=Bad cylinder
0708	CPU clock too fast in fast speed		Z=7=DMA overrun
0709	Failed to switch bus clock to ATCLK		Z=8=ID CRC error
110X	Timer X (0-2) failed to register test		Z=9=Data CRC error
1200	Memory refresh signal stuck high		Z=A=End of cylinder
1201	Memory refresh signal stuck low		Z=B=Unrecognizable error
211X	DMA 1 failed R/W test at register x (0-7)	A001	No 80287 detected
212X	DMA 2 failed R/W test at register x (0-7)	A002	80287 failed stack register R/W test
221X	Bad DMA page register; X=register 0-7	A00C	No zero-divide interrupt from 80287
300X	HP-HIL controller failed self test; X=data	AF00	Weitek coprocessor didn't enter protected mode
	X = xxx1 = > R/W fail with data = 0DA5Ah	AF01	Weitek coprocessor nor present
	X = xx1x = > R/W fail with data = 0DA5Ah	AF02	Weitek coprocessor fails register test
	X = x1xx = > R/W fail with data = 0DA5Ah	AF05	Weitek coprocessor fails addition test
	X = 1xxx = > R/W fail with data = 0DA5Ah	AF06	Weitek coprocessor fails interrupt test
3010	HP-HIL device test failed	AF0C	Weitek coprocessor fails interrupt test
4XYZ	Lower 640K failed R/W test;	CXYZ	R/W error on extended RAM in XY bank
	X=0,2,4,6 Y>0=Bad U23 Z>0=Bad U13		X = 0 = > Even byte bad
	X=1,3,5,7 Y>0=Bad U43 Z>0=Bad U33		X = 1 = > Odd byte bad
	X=8 Y>0=Bad U22 Z>0=Bad U12		XY = 64K bank where RAM failed
	X=9 Y>0=Bad U42 Z>0=Bad U32	CFFF	No extended RAM found
61XY	RAM address line XY stuck	EXYZ	Extended RAM marching 1s failure at XYZ
	Some address lines to RAM stuck to 0 or 1		X = 0 = > Byte 0 is bad
	XY = 00bb bbbb = > line bbbbbb is stuck		X = 1 = > Byte 1 is bad
	XY = 01bb bbbb = > Multiple address lines are stuck bbbbbb is the first bad one		X = 2 = > Byte 2 is bad
			X = 3 = > Byte 3 is bad

Pavilion Series 3100 & 8000

Code	Meaning	Code	Meaning
02	Verify real mode	7C	Set up hardware interrupt vectors
03	Disable NMI	7E	Initialize coprocessor, if present
04	Get processor type	80	Disable onboard super I/O ports
06	Initialize system hardware	81	Late POST device initialization
08	Initialize chipset with POST values	82	Detect & install external RS-232 ports
09	Set IN-POST flags	83	Configure non-MDC IDE controllers
0A	Initialize CPU registers	84	Detect & install external parallel ports
0B	Enable CPU registers	85	Initialize PnP ISA devices
0C	Initialize cache to POST values	86	Reinitialize onboard I/O ports
0E	Initialize I/O component	87	Set motherboard configurable devices
0F	Initialize local IDE bus	88	Initialize BIOS data area
10	Initialize power management	89	Enable NMI's
11	Load alternate registers	8A	Initialize extended BIOS data area
12	Restore CPU control word during warm boot	8B	Test & initialize PS/2 mouse

Code	Meaning	Code	Meaning
13	Initialize PCI bus mastering devices	8C	Initialize floppy controller
14	Initialize keyboard controller	8F	Determine number of ATA drives
16	BIOS ROM checksum	90	Initialize hard disk controllers
17	Initialize cache before memory size	91	Initialize local BUS HD controllers
18	Initialize 8254 timer	92	Jump to user patch 2
1A	Initialize DMA controller	93	Build MPTABLE for multiprocessor boards
1C	Reset PIC	94	Disable A-20 line
20	Test DRAM refresh	95	Install CD-ROM for boot
22	Test 8742 keyboard controller	96	Clear huge ES segment register
24	Set ES segment register to 4GB	97	Fix up multiprocessor table
26	Enable A-20 line	98	Search for options ROM's
28	Autosize DRAM	99	Check for smart drive
29	Initialize POST memory manager	9A	Shadow ROM option
2A	Clear 512K base RAM	9C	Set up power management
2C	RAM address line failure	9E	Enable hardware interrupts
2E	RAM data failure, low byte	9F	Determine number of ATA & SCSI drives
2F	Enable cache before BIOS shadow	A0	Set time of day
30	RAM data failure, high byte	A2	Check key lock
32	Test CPU, BUS clock frequency	A4	Initialize typematic rate
33	Initialize POST dispatch manager	A8	Erase F2 prompt
34	Test CMOS RAM	AA	Scan for F2 keystroke
35	Initialize alternate chipset registers	AC	Enter SETUP
36	Warm start shut-down	AE	Clear IN-POST flag
37	Reinitialize chipset (MB only)	B0	Check for errors
38	Shadow system BIOS ROM	B2	POST done, prepare for boot
39	Reinitialize cache (MB only)	B4	One short beep before boot
3A	Autosize cache	B5	Terminate quiet boot
3C	Configure advanced chipset registers	B6	Check password (optional)
3D	Load alternate registers new CMOS values	B8	Clear global descriptor table
40	Set initial CPU speed	B9	Clean up all graphics
42	Initialize interrupts	BA	Initialize DMI parameters
44	Initialize BIOS interrupts	BB	Initialize PnP option ROM's
45	POST device initialization	BC	Clear parity checkers
46	Check ROM copyright notice	BD	Display multi boot menu
47	Initialize manager for PCI option ROM's	BE	Clear screen optional
48	Check video config against CMOS	BF	Check virus and backup reminders
49	Initialize manager for PCI option ROM's	C0	Try to boot with Int 19
4A	Initialize all video adapters	C1	Initialize POST error manager
4B	Display quiet boot screen	C2	Initialize error logging
4C	Shadow video BIOS	C3	Initialize error display function
4E	Display BIOS copyright notice	C4	Initialize system error handler
50	Display CPU type & speed	E0	Initialize the chipset
51	Initialize	E1	Initialize the bridge
52	Test keyboard	E2	Initialize the processor
54	Set key click if enabled	E3	Initialize system timer
56	Enable keyboard	E4	Initialize system I/O
58	Test for unexpected interrupts	E5	Check force recovery boot
59	Initialize POST display service	E6	Checksum BIOS ROM
5A	Display "Press F2 to Enter Setup"	E7	Got to BIOS

Code	Meaning	Code	Meaning
5B	Disable CPU cache	E8	Set huge segment
5C	Test RAM, 512-640K	E9	Initialize multiprocessor
60	Test extended memory	EA	Initialize OEM special code
62	Test extended memory address lines	EB	Initialize PIC & DMA
64	Jump to user patch 1	EC	Initialize memory type
66	Configure advanced cache registers	ED	Initialize memory type
67	Initialize multi-processor APIC	EE	Shadow boot block
68	Enable external & processor caches	EF	System memory test
69	Set up SMM area	F0	Initialize interrupt vectors
6A	Display external L2 cache size	F1	Initialize runtime clock
6C	Display shadow area message	F2	Initialize video
6E	Display high address for UMB recovery	F3	Initialize beeper
70	Display error message	F4	Initialize BOOT
72	Check for configuration errors	F5	Clear huge segment
74	Test real time clock	F6	Boot to mini-DOS
76	Check for keyboard errors	F7	Boot to full DOS
7A	Test for key lock on		

IBM

Tests are performed by PC/XT/AT and PS/2 machines. There will be POST Codes (below), beep codes and screen displays if possible, but the XT does not give POST codes. ATs emit codes to 80h, while PS/2 models 25 and 30 emit to 90h, and 35 and above to 680. The BIOS will test main system components first, then non-critical ones. If there is an error, the BIOS will look for a reference diskette in drive A: so diagnostics can be performed.

IBM POST I/O Ports

Architecture	Typical Computer	Port
PC	PC	none
ISA	XT	60
	AT	80
	PS/2 25,30	90, 190
MCA	PS/2 50 up	680, 3BC
EISA	none	none

POST Procedures

Procedure	Meaning
CPU	Perform register test on the CPU by writing data patterns to the registers and reading the results of the write.
BIOS Checksum	The value of bits inside the BIOS chip(s) is added to a preset value that should create a total of 00.
CMOS RAM	RAM within the CMOS chip is tested by writing data patterns to the area and verifying that the data was stored correctly.
DMA	Test DMA chips by forcing control inputs to the CPU to an active state and verifying that the proper reactions occur.

Procedure	Meaning
8042/8742 Keyboard Controller	Test including Gate A20 and the reset command. The buffer space is prepared and data is sent to the determined area via the keyboard controller to see if commands are received and executed correctly.
Base 64K System RAM.	Perform a walking-bit test of the first 64K of RAM so the BIOS vector area can be initialised. Check for bad RAM chips or a data/address line.
8259A PIC	Determine if commands to interrupt CPU processes are carried out correctly. Check the PIC/PIT/RTC/CMOS or Clock chip(s).
8254 PIT	Check that proper setup and hold times are given to the PIC for interrupts of the CPU processes. Check the PIT or Clock chip.
82385 Cache Controller	This is normally responsible for cache and shadow memory.
CMOS RAM Configuration Data	Check information in CMOS RAM before further testing so any failures after this could also be down to the CMOS chip.
CRT controllers	Test any video adapters listed in the CMOS.
RAM above 64K	Perform a walking-bit test on memory above 64K listed in the CMOS.
Keyboard	Test interface to keyboard including scan code stuck keys etc.
Pointing Device (mouse etc)	Test and init vector for pointing devices. Failure to see a device may be the device itself but there may be a problem with the CMOS or 8042/8742.
Diskette Drive A:	Test and initialise the A: drive.
Serial Interface Circuitry	Test any RS232 devices found at the proper I/O address.
Diskette Controllers	If an A: drive has been found further testing is performed before proceeding to the bootloader. This test includes reading the first sector of any diskette in the drive to see if a valid boot code is there.
Fixed Disk Controllers	Test and initialise any hard drives set in the CMOS including reading the first sector of the hard drive to see if a valid boot code exists.

XT (Port 60)

The PC uses an irregular way of sending codes to ports 10 and 11, which is impractical to monitor on a POST card. The XT, on the other hand, uses three methods; before initializing the display, it issues a few codes to port 60 (the 8255 controller for the keyboard) for critical system board errors. It beeps to indicate successful or unsuccessful POST, and displays error messages. After initializing the display, it writes error codes to memory address 15, which are sent to the screen as part of other error messages.

Code	Meaning
00 or FF	CPU register test failed
01	BIOS ROM (ROS) checksum failed
02	Timer I failed
03	8237 DMA register write/read failed or unexpected timer 1 request for DMA ch 1
04	After enabling port 213 expansion box, base 32K memory write/read of AA, 55, FF, 01 and 00 test failed; POST output alternates between POST code and failing bit pattern.
	Size memory, init 8259 PIC, setup interrupt vectors in RAM, read configuration switches, poll jumper. If installed, load manufacturing test via keyboard port and run. If not, initialize rest of system.

AT POST Codes

Code	Meaning
00	Main board damaged
01	80286 test in real mode; verify read/write registers, flags and conditional jumps.
02	ROM checksum test-test 32K ROMs; POST BASIC and BIOS.
03	Test CMOS shutdown byte-rolling bit pattern and verified at shutdown address.
04	8254 timer 1; all bits on; set timer count; check all bits on.

Code	Meaning
05	8254 timer 1; all bits off; set timer count; check all bits off.
06	8237 DMA 0 init channel register test. Disable DMA controller; r/w current address to all channels
07	8237 DMA 1 init channel register test. Disable DMA controller; r/w current address to all channels
08	DMA page register test-r/w all page registers. Check 74LS612.
09	Storage refresh test. 8042 i/face test I/O issue self test; check 55H received
0A	Keyboard controller test 1; Soft reset
0B	Keyboard controller test 2; Reset 8042
0C	Keyboard controller test 3; Test switch settings
0D	Keyboard controller test 4: Write byte 0 of 8042 mem; issue comd to 8042, await response.
0E	Base 64K r/w memory test-r/w data patterns AAh, 55h.
0F	Get I/P buffer switch setting. Also Base 64K r/w memory test #2-r/w data patterns AAh, 55h.
10	Roll error code to MFG Port
11	Initialise display row count. Verify 286 LGDT.SGDT LIDT/SIDT instruction
12	Protected mode register test failure
13	Initialise 8259
14	Setup interrupt vector to temp interrupt
15	Establish BIOS interrupt call subroutine vectors. CMOS checksum/battery OK
16	Set data segment or Check CMOS battery condition.
17	Set defective battery flag or CMOS checksum error.
18	Ensure CMOS dividers set or enable protected mode.
19	Set return address byte in CMOS.
1A	Set temporary stack or protected mode test. Determine memory size; verify parity.
1B	Segment address 01-0000 (second 64K memory test)
1C	Set or reset; check 512-640 memory installed
1E	Set (expanded?) memory size determined in CMOS; or determine memory size above 1024K.
1F	Test address lines 19-23
20	Fatal addressing error; Shutdown.
21	Return 1 from shutdown. Initialise and start CRT controller (6845); test video r/w; test video enable; select alpha mode; w/r patterns; or check CMOS config data.
22	Enable video signal and set mode; CRT interface test; verify video enable and horizontal sync. Video card init failure or invalid switch setting.
23	Check for advanced video card; Video card initialisation failure or invalid switch setting.
24	8259 PIC test -r/w interrupt mask register with 1s and 0s; mask device interrupts off.
25	Check for hot interrupts; test interrupt mask registers.
26	Display 101 error; Check for unexpected interrupts.
27	Check the converting logic (106 error)
28	Check hot NMI interrupts (error 107)
29	Test data bus to timer 2 (error 108). 8253 timer register failure.
2A	8253 Timer speed failure (error 102)
2B	Too fast; or 8253 Timer interrupt initialisation.
2C	Too slow; or Timer 0 interrupt failure (error 103)
2D	Check 8042 (k/b controller) for last command excepted (error 105)
2F	Check for warm boot
30	Set shutdown return 2; Protected mode r/w memory test step 1.
31	Enable protected mode; Protected mode r/w memory test step 2.
32	Address lines 0-15
33	Next block of 64K; Protected mode r/w memory test step 3.
34	Restore checkpoint; Protected mode r/w memory test step 4.
35	Keyboard test; Check for manufacturing burn in test.

Code	Meaning
36	Check <AA> scan code; keyboard clock error.
38	Error-check 8042 working; also 37 and 39
3A	Initialise 8042; keyboard locked
3B	Check for ROM in 2K blocks
3C	Check for floppy diskette drive
3D	Initialise floppy for drive type
3E	Initialise hard drive
3F	Initialise printer; non-fatal error; press F1 to continue.

Additional Protected Mode Tests

Code	Meaning
40	Enable hardware interrupt if 80287; initialisation
41	System code @ segment code E000.0
42	Exit to system code
43	Go to boot loader diskette attachment test
44	Boot from fixed disk
45	Unable to boot; go to BASIC
81	Build descriptor table
82	Switch to virtual mode
90-B6	EXEC_00 to EXEC_31 & SYS_32 to SYS_38 tests; memory test; boot loader.
DD	Transmit error code to MFG_PORT
F0	Set data segment
F1	Interrupt test (programming interrupt 32)
F2	Exception interrupt test
F3	Verify 286 LDT/SDT and LTR/STR instructions.
F4	Verify 286 bound instruction
F5	Verify push and pop all instruction; stack/register test.
F6	Verify access rights function correctly.
F7	Verify Adjust RPL field of selector instructions (ARPL) functions
F8	Verify LAR function
F9	Verify LSL i(Load Segment Limits) instruction
FA	Low meg chip select test

PS/2 (Micro Channel) POST Codes

Code	Meaning
00	CPU test; FFAA0055 pattern
01	32 bit CPU register test; setup system timer
02	System ROM checksum
03	Test system enable/system port 94 enable/check
04	Test system POS register; port 102 enable/check
05	Test adapter setup port; POS port 96 enable/check
06	Test RTC/CMOS shutdown byte; Byte 0F CMOS (NMI disable)
07	Test extended CMOS location; ports 74-76 test
08	Test DMA & page register 8 channels; ports 2
09	Initialise DMA command & mode registers
0A	Test refresh (port 61)

Code	Meaning
0B	Test keyboard controller buffers (8042-port 61
0C	Keyboard controller self test (8042-port 60)
0D	Keyboard controller test continuation (8042)
0E	Keyboard self test error indicated (port 64)
0F	Setup system memory configuration
10	Test first 512K RAM in real mode
11	Half system if memory test error
12	Verify LGDT/SGDR LIDT/SIDT (keyboard commands)
13	Initialise PIC #1 (Master)
14	Initialise PIC #2 (Slave)
15	Initialise A20 interrupt vectors
16	Setup extended vector table
17	Check power RTC/CMOS power good signal (byte 0D)
18	Check RTC/CMOS checksum
19	RTC/CMOS lost power (0D 80h)
1A	Skip memory test in protected mode if warm reset
1B	Prepare for shutdown; protected mode initialisation
1C	Setup stack pointer point to the end of first 64K
1D	Decide low memory size in protected mode; Size base memory
1E	Save memory size detected
1F	Setup system memory split address
20	Check for extended memory beyond 64 Mb
21	Test memory address bus lines
22	Clear parity error and channel check; Disable NMI
23	Initialise interrupt 00; system timer
24	Determine CMOS validity
25	Write keyboard controller (8042) command byte
40	Check valid CMOS and video
41	Display error code 160. Check CMOS, AC ripple.
42	Test PIC #1 & PIC #2 registers; Master/Slave test
43	Test PIC #1 & PIC #2 registers with another pattern
44	Check for interrupt with interrupt masked; check for NMI when disabled.
45	Test NMI
46	NMI error detected
47	Test system timer 0
48	Check stuck speaker clock; speaker bitstuck test
49	Test timer 0 count
4A	Test timer 2 output
4B	Check if timer interrupt occurred
4C	Test timer 0 for count too fast or slow
4D	Verify timer 0 interrupt
4E	Check 8042 ready for command; buffer free
4F	Check for soft reset
50	Prepare for shutdown/protected mode
51	Start protected mode test
52	Test memory in 64K increments
53	Check if memory test done
54	Shutdown system and return to real mode
55	Test for manufacture or regular test; test for loop. Check jumper.

Code	Meaning
56	Disable keyboard
57	Check for keyboard self test
58	Keyboard test passed; check for errors
59	Test keyboard interface
5A	Initialise mouse
5B	Disable mouse
5C	Initialise interrupt vectors
5D	Initialise interrupt vectors
5E	Initialise interrupt vectors
5F	BIOS data area
60	Determine diskette rate
61	Reset floppy controller/drive
62	Floppy drive test
63	Turn floppy motor off
64	Serial port setup
65	Enable/test RTC interrupt
66	Configure floppy drives
67	Configure hard drive
68	Enable system CPU arbitration; wait states
69	Scan for optional ROMs
6A	Verify serial and parallel ports
6B	Setup equipment byte
6C	Setup configuration errors reported
6D	Set keyboard typematic rate
6E	Reset page register; boot up system (Int 19 bootloader)
70	Reset disk
71	Read bootcode for E6/E9
72	Control to bootcode
73	Bootcode/ROM Basic

INTEL

CA810E

Also RC440BX & SR 440BX. Possibly based on AMI.

Code	Meaning
D0	NMI disabled. Keyboard controller and RTC enabled. Initialization code checksum verification starting
D1	Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode
D3	Initialize chipset, start memory refresh, and determine memory size
D4	Verify base memory
D5	Initialization code to be copied to segment 0 and control to be transferred to segment 0
D6	Control is in segment 0. Used to check if in recovery mode and verify main BIOS checksum. If in recovery mode or if checksum is wrong, go to E0 for recovery. Othewise, got o D7 to give control to main BIOS
D7	Find main BIOS module in ROM image
D8	Uncompress the main BIOS module
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM

Boot Block Recovery Code Checkpoints

Code	Meaning
E0	Onboard diskette controller (if any) is initialized. Compressed recovery code is uncompressed at F000:0000 in shadow RAM. Give control to recovery code at F000 in shadow RAM. Initialize interrupt vector tables, system timer, DMA controller, and interrupt controller
E8	Initialize extra (Intel recovery) module
E9	Initialize diskette drive
EA	Try to boot from diskette. If reading of boot sector is successful, give control to boot sector code
EB	Boot from diskette failed; look for ATAPI (LS-120, Zip) devices
EC	Try to boot from ATAPI device. If reading boot sector is successful, give control to boot sector code
EF	Boot from diskette and ATAPI device failed. Give2 beeps. Retry booting procedure (go to checkpoint E9)

Runtime Code Uncompressed in F000 Shadow RAM

Code	Meaning
03	NMI is disabled. To check soft reset/power on
05	BIOS stack set. Going to disable cache if any
06	POST code to be uncompressed
07	CPU init and CPU data area init to be done
08	CMOS checksum calculation to be done next
0B	Any initialization before keyboard BAT to be done next
0C	Keyboard controller I/B free. To issure the BAT command to the keyboard controller
0E	Any initialization after keyboard controller BAT to be done next
0F	Keyboard command byte written
10	Going to issue Pin 23, 24 blocking/unblocking command
11	Going to check pressing of <INS>, <END> key during power-on
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and interrupt controllers
13	Video display is disabled and port B is initialized. Chipset init about to begin
14	8254 timer test about to start
19	About to start memory refresh test
1A	Memory refresh line is toggling. Going to check 15 µs On/OFF time
23	To read 8042 input port and disable megakey GreenPC feature. make BIOS cade segment writeable
24	To do any setup before int vector init
25	Interrupt vector initialization to begin. To clear password if necessary
27	Any initialization before setting video mode to be done
28	Going for monochrome mode and color mode setting
2A	Different buses init (system, static, output devices) to start if present
2B	To give control for any setup required before optional ROM check
2C	To look for optional video ROM and give control
2D	To give control to do any processing after video ROM returns control
2E	If EGA/VGA not found then do display memory R/W
2F	EGA/VGA not found. Display memory R/W test about to begin
30	Display memoryR/W test passed. About to look for the retrace checking
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test
32	Alternate Disaply memory R/W test passed. To look for the alternate display retrace checking
34	Video display checking over. Display mode to be set next
37	Display mode set. Going to display the power on message
38	Different buses init (input, IPL, general devices) to start if present

Code	Meaning
39	Display different buses initialization error messages
3A	New cursor position read and saved. To display the Hit <DEL> message
40	To prepare the descriptor tables
42	To enter virtual mode for memory test
43	To enable interrupts for diagnostics mode
44	To initialize data to check memory wrap around at 0:0
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system test memory
46	Memory wrap around test done. Size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640KB memory
48	Patterns written in base memory. Going to find out amount of memory below 1M memory
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4E)
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M
4D	memory above 1M cleared (SOFT RESET) Going to save the memory size (Go to checl point # 52
4E	Memory test started. (NOT SOFT RESET) About to display the first 64KB memory size
4F	Memory size display started. Will be updated during memory test. going for sequential and random memory test
50	Memory testing/iniialization below 1MB complete. Adjust displayed memory size for relocation shadow
51	Memory size display adjusted due to relocation/shadow. Memory test above 1MB to follow
52	Memory testing/initialization above 1MB complete. Going to save memory size information
53	Memory size information is saved. CPU registers are saved. Going to enter real mode
54	Shutdown successful, CPu in real mode. Going to disable gate A20 line and disable parity/NMI
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow
58	Memory size adjusted for relocation/shadow. Going to clear hit <DEL> message
59	Hit <DEL> message cleared. <WAIT...> message displayed. Start DMA and interrupt controller test
60	DMA page register test passed. To do DMA #1 base register test
62	DMA #1 base register test passed. To do DMA #2 base register test
65	DMA #2 base register test passed. To program DMA #1 and #2
66	DMA #1 and #2 programming over. To initialize 8259 interrupt controller
7F	Extended NMI sources enabling is in progress
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command
82	Keyboard controller interface test over. To write command byte and init circular buffer
83	Command byte written, global data init done. To check for lock-key
84	Lock key checking over. to check for memory size mismatch with CMOS
85	Memory size check done. to display soft error and check for password or bypass setup
86	Passwoed checked. About to do programming before setup
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup
89	Programming after setup complete. Going to display power-on screen message
8B	First screen message. <WAIT...> message. PS/2 mouse check and extended BIOS data area allocation
8C	Setup options programming after CMOS setup about to start
8D	Going to hard disk controller reset
8F	Hard disk controller reset done. Floppy setup to be done next
91	Floppy setup complete. Hard disk setup to be done next
95	Init of different buses optional ROMs from C800 to start.
96	Going to do any init before C800 optional ROM control
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next

Code	Meaning
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache
99	Iinitialization after optional ROM test over. Going to setup timer data area and printer base address
9A	Return after setting timer and printer base addresses. Going to set the RS-232 base address
9B	Returned after RS-232 base address. Going to do any initialization before coprocessor test
9C	Required initialization before coprocessor is over. Going to initializae the coprocessor test
9D	Coprocessor initialized. Goin to do any initialization after coprocessor test
9E	Initialization after copro test is complete. Goin to check extended keyboard, keyboard ID and num-lock
A2	Going to display any soft errors
A3	Soft error display complete. Going to set keyboard typematic rate
A4	Keyboard typematic rate set. To program memory wait states
A5	Going to enable parity/NMI
A7	NMI and parity enabled. Initialization required before giving control to optional ROM at E000
A8	Initialization before E000 ROM control over. E000 ROM to get control next
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration
AB	Put Int13 module runtime image to shadow
AC	Generate MP for multiprocessor support (if present)
AD	Put CGA Int10 module (if present) in shadow
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow
B1	Going to copy any code to specific area
00	Copying of code to specific area done. Going to give control to Int19 boot loader

440 Series

Code	Meaning	Code	Meaning
02	Verify real mode	82	Detect and install external RS232 ports
03	Disable non-maskable interrupt (NMI)	83	Configure non-MCD IDE controllers
04	Get processor type	84	Detect and install external parallel ports
06	Initialize system hardware	85	Initialize PC compatible PnP ISA devices
08	Initialize chipset with initial POST values	86	Reinitialize onboard I/O ports
09	Set IN POST flag	87	Set motherboard configurable devices
0A	Initialize processor registers	88	Initialize BIOS Data Area
0B	Enable processor cache	89	Enable non-maskable interrupts (NMI)
0C	Initialize caches to initial POST values	8A	Initialize extended BIOS data area
0E	Initialize I/O component	8B	Test and initialize PS/2 mouse
0F	Initialize the local bus IDE	8C	Initialize diskette controller
10	Initialize power management	8F	Determine number of ATA drives
11	Load alternate registers initial POST values	90	Initialize hard disk controllers
12	Restore proc control word in warm boot	91	Initialize local bus hard disk controllers
13	Initialize PCI bus mastering devices	92	Jump to UserPatch2
14	Initialize keyboard controller	93	Build MPTABLE for multiprocessor boards
16	BIOS ROM checksum	94	Disable A20 address line
17	Initialize cache before memory autosize	95	Install CD-ROM for boot
18	8254 timer initialization	96	Clear huge ES segment register
1A	8237 DMA controller initialization	97	Fix up multiprocessor table
1C	Reset programmable interrupt controller	98	Search for option ROMs
20	Test DRAM refresh	99	Check for SMART drive
22	Test keyboard controller	9A	Shadow option ROMs

Code	Meaning	Code	Meaning
24	Set ES segment register to 4GB	9C	Setup power management
26	Enable A20 line	9E	Enable hardware interrupts
28	Autosize DRAM	9F	Determine number of ATA and SCSI drives
29	Initialize POST memory manager	A0	Set time of day
2A	Clear 512KB base RAM	A2	Check key lock
2C	RAM failure on address line xxxx	A4	Initialize typematic rate
2E	RAM failure on bits xxxx of low byte	A8	Erase F2 prompt
2F	Enable cache before system BIOS shadow	AA	Scan for F2 key stroke
30	RAM failure on bits xxxx of high byte	AC	Enter SETUP
32	Test processor bus-clock frequency	AE	Clear IN POST flag
33	Initialize POST dispatch manager	B0	Check for errors
34	Test CMOS RAM	B2	POST done - prepare to boot system
35	Initialize alternate chipset registers	B4	One short beep before boot
36	Warm start shut down	B5	Terminate QuietBoot
37	Reinitialize the chipset (motherboard only)	B6	Check password (optional)
38	Shadow system BIOS ROM	B8	Clear global descriptor table
39	Reinitialize the cache (motherboard only)	B9	Clean up all graphics
3A	Autosize cache	BA	Initialize DMI parameters
3C	Configure advanced chipset registers	BB	Initialize PnP Option ROMs
3D	Load alternate registers with CMOS values	BC	Clear parity checkers
40	Set initial processor speed new	BD	Display MultiBoot menu
42	Initialize interrupt vectors	BE	Clear screen (optional)
44	Initialize BIOS interrupts	BF	Check virus and backup reminders
45	POST device initialization	C0	Try to boot with Int19h
46	Check ROM copyright notice	C1	Initialize POST Error Manager (PEM)
47	Initialize manager for PCI option ROMs	C2	Initialize error logging
48	Check video configuration against CMOS	C3	Initialize error display function
49	Initialize PCI bus and devices	C4	Initialize system error handler
4A	Initialize all video adapters in system	D0	Interrupt handler error
4B	Display QuietBoot screen	D2	Unknown interrupt error
4C	Shadow video BIOS ROM	D4	Pending interrupt error
4E	Display BIOS copyright notice	D6	Initialize option ROM error
50	Display processor type and speed	D8	Shutdown error
51	Initialize EISA motherboard	DA	Extended Block Move
52	Test keyboard	DC	Shutdown 10 error
54	Set key click if enabled	E0	Initialize the chipset
56	Enable keyboard	E1	Initialize the bridge
58	Test for unexpected interrupts	E2	Initialize the processor
59	Initialize POST display service	E3	Initialize system timer
5A	Display prompt "Press F2 to enter "SETUP"	E4	Initialize system I/O
5B	Disable processor cache	E5	Check force recovery boot
5C	Test RAM between 512 and 640KB	E6	Checksum BIOS ROM
60	Test extended memory	E7	Go to BIOS
62	Test extended memory address lines	E8	Set huge segment
64	jump to UserPatch1	E9	Initialize multiprocessor
66	Configure advanced cache registers	EA	Initialize OEM special code
67	Initialize multiprocessor APIC	EB	Initialize PIC and DMA
68	Enable external and processor caches	EC	Initialize memory type
69	Setup SMM area	ED	Initialize memory speed

Code	Meaning	Code	Meaning
6A	Display external L2 cache size	EE	Shadow boot block
6C	Display shadow area message	EF	System memory test
6E	Display possible high address for UMB recovery	F0	Initialize interrupt vectors
70	Display error messages	F1	Initialize runtime clock
72	Check for configuration errors	F2	Initialize video
74	Test real-time clock	F3	Initialize beeper
76	Check for keyboard errors	F4	Initialize boot
7A	Test for key lock on	F5	Clear huge segment
7C	Setup hardware interrupt vectors	F6	Boot to mini-DOS
7E	Disable onboard Super I/O ports and IRQs	F7	Boot to full DOS
81	Late POST device initialization		

440GX

Codes in Execution Sequence.

Code	Meaning
02	Verify real mode
12	Restore processor control word during warm boot (only occurs on warm boot)
24	Set ES segment register to 4GB
04	Get processor type
06	Initialize system hardware
18	8254 timer initialization
08	Initialize PCIset registers with initial POST values
C4	Initialize system flags in CMOS
11	Load alternate registers with initial POST values
0E	Initialize I/O
0C	Initialize caches to initial POST values
16	BIOS ROM checksum
17	Turn cache off
28	Autosize DRAM
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus (1st 4Meg)
2F	Initialize L2 cache if enabled in CMOS
38	Shadow system BIOS ROM
20	Test DRAM refresh
29	Post Memory Manager initialization (PMM)
33	Post Dispatch Manager initialization
34	Test CMOS
C1	Post error manager initialization
09	Set IN POST flag
0A	Initialize processor registers and processor microcode
3A	Autosize cache
0B	Enable processor cache
0F	Initialize the local bus IDE (not used anymore but here for Phoenix standard)
10	Initialize Power Management (APM not used in L440GX+)
14	Initialize keyboard controller
1A	8237 DMA controller initialization

Code	Meaning
1C	Reset programmable interrupt controller (PIC)
22	Test 8742 keyboard controller
32	Read processor bus-clock frequency and compute boot processor speed
67	Initialize and register via SMM through APIC bus
69	Initialize SMI handler for all processors
00	Wait for secondary processor to execute init SMI handler
F4	Exit SMI handler (secondary processor executed halt in SMI)
3C	Configure advanced PCIset registers and reset coprocessor
3D	Load alternate registers with CMOS values
42	Initialize interrupt vectors
46	Check ROM copyright notice
45	Initialize all pre-PnP devices
49	Initialize PCI bus and devices (also read ESCD and allocate resources)
48	Check video configuration against CMOS (VGA or MDA)
4A	Initialize all video adapters in system
4C	Shadow video BIOS ROM
24	Put processor in big real mode (flat mode memory addressing - up to 4GB)
59	Post display manager initialization (video screen error codes now visible)
22	Reset and test keyboard first try (only warm reset)
52	Reset and test keyboard controller (both warm and cold reset)
54	Set key click if enabled
76	Enable keyboard
58	Test for unexpected interrupts
4B	QuietBoot start (not used in L440GX+)
4E	Display copyright notice
50	Display processor(s) type and speed
51	EISA init (not used in L440GX+)
5A	Display prompt "Press F2 to enter SETUP"
5B	Disable processor L1 cache for memory test
5C	Test RAM between 512KB and 640KB
60	Test extended memory (4MB to top of memory)
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache registers
68	Enable external and processor caches
6A	Display external cache size
6C	Display shadow message
6E	Display non-disposable segments
70	Display error messages to video
72	Check for configuration errors
74	Test real time clock
7C	Setup hardware interrupt vectors
7E	Test coprocessor if present
80	Not used
88	Initialize BIOS Data Area, time-outs for detecting parallel, serial and HDD controller. Clear CMOS shutdown flag
8A	Initialize Extended BIOS Data Area
81	Late POST core initialization of devices
87	Configure MCD devices

Code	Meaning
85	Initialize and detect PC compatible PnP ISA devices (parallel, serial, etc..)
82	Not used
84	Clear interrupts from COM port detection
86	Console redirection initialized
83	Configure onboard hard disk controller
89	Enable NMI
8C	Initialize floppy controller
90	Initialize and detect hard disks
8B	Detect and test for mouse and auxiliary device on keyboard controller
95	Install CD-ROM for boot
92	Jump to UserPatch2
C5	Initialize GPNV areas in DMI
98	Search for option ROMs. One long, two short beeps on checksum failure of an option ROM
93	Scan for User Flash ROMs. MP Table initialization (wake up secondary processor and halt it)
9C	Setup Power Management (not used)
9D	Enable security
9E	Enable hardware interrupts
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
C2	Initialize DMI tables
C3	Log post errors with POST error manager and to SEL in BMC. Update VID bits and memory presence to BMC. Display and FRB errors (watchdog time-outs, bits or processor failures)
A8	Erase F2 prompt
AA	Scan for F2 keystroke
AC	Initialize EMP port if selected. Remove COM2 from BDA if EMP is enabled. Enter SETUP
AE	Clear IN POST flag
B0	Secure boot if enabled (secure front panel, blank video, floppy write protect). Check for errors
B2	POST done - prepare to boot Operating System
B4	One short beep before boot
B5	Display QuietBoot (not used)
BE	Clear screen
B6	Check password (optional)
BC	Clear parity checkers
BA	Not used
B7	ACPI configuration (table configuration in memory and BDA)
BD	Display MultiBoot menu if ESC is hit
BF	Display system config summary (if enabled in CMOS)
8F	Get total # of hard drives and put in BDA
91	Program IDE hard drives (timing, PIO modes, etc...)
9F	Save total # of hard drives (SCSI and ATA) in BDA
97	Fixup MP table (checksum)
99	Check SMART hard drive
C7	Prepare to boot to OS. Clean up graphics and PMM areas
C0	Try to boot with Int19h. Return to video mode 3, disable PMM, return to real mode, disable gate A20, clears system memory, resets stack, invokes Int19h
D0	Interrupt handler error
D2	Unknown interrupt error
D4	Pending interrupt error

Code	Meaning
D6	Initialize option ROM error
D8	Shutdown error
DA	Extended Block Move
DC	Shutdown 10 error

440BX

Codes in Execution Sequence.

Code	Meaning
02	Verify real mode
12	Restore processor control word during warm boot (only occurs on warm boot)
24	Set ES segment register to 4GB
04	Get processor type
06	Initialize system hardware
18	8254 timer initialization
08	Initialize PCIset registers with initial POST values
C4	Initialize system flags in CMOS
11	Load alternate registers with initial POST values
0E	Initialize I/O
0C	Initialize caches to initial POST values
16	BIOS ROM checksum
17	Turn off cache
28	Autosize DRAM
2A	Clear 512KB base RAM
2C	RAM failure on address line xxxx
2E	RAM failure on data bits xxxx of low byte of memory bus (first 4 meg)
2F	Initialize L2 cache if enabled in CMOS
38	Shadow system BIOS ROM
20	Test DRAM refresh
29	Post Memory Manager initialization (PMM)
33	Post Dispatch Manager initialization
34	Test CMOS
C1	Post error manager initialization
09	Set IN POST flag
0A	Initialize processor registers and CPU microcode
3A	Autosize cache
0B	Enable processor cache
0F	Initialize the local bus IDE
10	Initialize Power Management (APM not used in Nightshade)
14	Initialize keyboard controller
1A	8237 DMA controller initialization
1C	Reset Programmable Interrupt Controller
22	Test 8742 Keyboard Controller
32	Read processor bus-clock frequency and compute boot processor speed
67	Initialize and register other CPU via SMM through APIC bus
69	Initialize SMI handler for all processors
00	Wait for secondary processor to execute init SMI handler
F4	Exit SMI handler (secondary processor executed halt in SMI)

Code	Meaning
3C	Configure advanced PCIset registers and reset coprocessor
3D	Load alternate registers with CMOS values
42	Initialize interrupt vectors
46	Check ROM copyright notice
45	Initialize all pre-PnP devices
49	Initialize PnP bus and devices (also read ESCD and allocate resources)
48	Check video configuration against CMOS (VGA or MDA)
4A	Initialize all video adapters in system
4C	Shadow video BIOS ROM
24	Put CPU in big real mode (flat mode memory addressing - up to 4GB)
59	Post display manager initialization (video screen error codes now visible)
22	Reset and test keyboard first try (only warm reset)
52	Reset and test keyboard controller (both warm and cold reset)
54	Set key click if enabled
76	Enable keyboard
58	Test for unexpected interrupts
4B	QuietBoot start (not used in N440BX)
4E	Display copyright notice
50	Display CPU(s) type and speed
51	EISA initialized (not used in N440BX)
5A	Display prompt "Press F2 to enter SETUP"
5B	Disable CPU L1 cache for memory test
5C	Test RAM between 512KB and 640KB
60	Test extended memory (4MB to top of memory)
62	Test extended memory address lines
64	Jump to UserPatch1
66	Configure advanced cache registers
68	Enable external and processor caches
6A	Display external cache size
6C	Display shadow message
6E	Display non-disposable segments
70	Display error messages to video
72	Check for configuration errors
74	Test real time clock
7C	Setup hardware interrupt vectors
7E	Test coprocessor if present
80	Not used
88	Init Data Area, time-outs for detecting parallel, serial and HD controller. Clear shutdown flag
8A	Initialize Extended BIOS Data Area
81	Late POST core initialization
87	Configure MCD devices
85	Initialize and detect PC compatible PnP ISA devices (serial, parallel, etc.)
82	Not used
84	Clear interrupts from COM port detection
86	Console redirection initialized
83	Configure onboard hard disk controller
89	Enable NMI
8C	Initialize floppy controller
90	Initialize and detect hard disks

Code	Meaning
8B	Detect and test for Mouse or Auxiliary device on keyboard controller
95	Install CD-ROM for boot
92	Jump to UserPatch2
C5	Initialize GPNV areas of DMI
98	Search for option ROMs. One long, two short beeps for checksum failure of an option ROM
93	Scan for User flash ROMs. MP Table initialization (wake up secondary processor and halt it)
9C	Setup Power Management (not used)
9D	Enable security
9E	Enable hardware interrupts
A0	Set time of day
A2	Check key lock
A4	Initialize typematic rate
C2	Initialize DMI tables
C3	Log POST errors and to SEL in BMC. Update VID bits and memory presence to BMC. Display any FRB errors (watchdog time-outs, bits or CPU failures)
A8	Erase F2 prompt
AA	Scan for F2 keystroke
AC	Initialize EMP port if selected. Remove COM2 from BDA of EMP is enabled. Enter SETUP
AE	Clear IN POST flag
B0	Turn on secure boot if enabled (secure front panel, blank video, floppy WP). Check for errors
B2	POST done - prepare to boot Operating System
B4	One short beep before boot
B5	Display QuietBoot (not used)
BE	Clear screen
B6	Check password (optional)
BC	Clear parity checkers
BA	Not used
B7	ACPI configuration (table configuration in memory and BDA)
BD	Display MultiBoot menu if ESC is hit
BF	Display system configuration summary (if enabled in CMOS)
8F	Get total # of hard drives and put in BDA
91	Program IDE hard drives (timing, PIO modes, etc.)
9F	Save total # of hard drives (SCSI and ATA) in BDA
97	Fixup MP Table (checksum)
99	Check SMART harddrive
C7	Prepare to boot OS, clean up graphics and PMM areas
C0	Try to boot Int19h. Return to video mode 3, disable PMM, return to real mode, disable gate A20, clear system memory, reset stack, invoke Int19h

OR840

Port 80	Port 81	Description
01		Transition to protected mode complete
	30	Seek relevant processor patch
	31	Apply processor patch
	32	Setup ICH GPIO base, SIO PME base, miscellaneous ICH settings
	33	Setup ICH and SIO GPIO attributes and values
	3A	Set ICH GPIO attributes and values
	3B	Set SIO GPIO attributes for GPIO10-17

Port 80	Port 81	Description
	3C	Set SIO GPIO attributes for GPIO20-27
	3D	Set SIO GPIO attributes for GPIO30-37
	3E	Set SIO GPIO attributes for GPIO40-43
	3F	Set SIO GPIO attributes for GPIO50-57
	40	Set SIO GPIO attributes for GPIO60-61
	41	Set initial values for SIO GPIOs
	34	SMBUS initialization
	35	Initialize L1 cache for use as memory during memory initialization
02		Start Minimum memory establishment
	00	Memory not supported (Not RDRAM)
	01	Memory not supported (SPD contains invalid width - not 16 or 18)
	02	No memory devices were found on one or both channels
	03	More than 32 devices on the channel
	04	Memory failure (number of devices detected does not match SPD data)
	05	Memory not supported (FRAS data in SPD is invalid)
	0A	Memory not supported (Populated memory requires too many time domains)
	0B	Memory not supported (No valid channel frequency)
	0C	Memory failure (levelization failure 0 ran out of time domains)
	0D	Memory not supported (unsupported memory technology)
	0E	Memory failure (Continuity module missing or chipset failure)
	0F	Memory not supported (could no find valid refresh rate
	10	Memory not supported (invalid refresh information in SPD
	11	Memory not supported (TCDC invalid)
	12	Memory not supported (does not support enough time domains)
	13	Memory not supported (TRDC invalid)
	14	Memory not supported (invalid SPD TCLS or TCAS)
	15	Memory not supported (SPD mismatch between channel A and B)
	17	Memory not supported (SPD mismatch between channel A and B)
	18	Memory not supported (SPD mismatch between channel A and B)
	19	Memory not supported (SPD mismatch between channel A and B)
	1A	Memory not supported (SPD mismatch between channel A and B)
	1B	Memory not supported (SPD mismatch between channel A and B)
	1C	Memory not supported (SPD mismatch between channel A and B)
	1F	Memory not supported (SPD mismatch between channel A and B)
	20	Memory not supported (invalid number of devices on RIMM)
	22	Memory not supported (SPD mismatch between channel A and B)
	24	Memory failure (Detected bad chipset configuration)
	25	Memory not supported (RIMMs must support ECC)
	28	Memory not supported (unsupported memory technology)
	29	Memory not supported (unsupported memory technology)
	2A	Memory not supported (could not find valid CAS latency)
	2C	Memory not supported (can not mix registered and non-registered memory
	2D	Memory not supported (could not find valid CAS latency)
	2E	Memory failure (levelization phase 1)
	2F	Memory failure (levelization phase 2)
	38	Start memory discovery
	40	STEP: Setup for memory discovery
	41	STEP: SIO reset
	42	STEP: Serial enumeration

Port 80	Port 81	Description
	44	RDRAM STEP: Detect RIMM presence using SPD
	45	RDRAM STEP: DRCG bypass mode - SIO RESET/SET RESET/CLEAR RESET
	46	RDRAM STEP: Determine RAMBUS frequency and set DRCG
	47	RDRAM STEP: MCH RAC initialization
	48	RDRAM STEP: Page Policy and power management (initialization mode)
	4A	RDRAM STEP: Test 77
	4B	RDRAM STEP: Serial enumeration
	4C	RDRAM STEP: Group enumeration
	4D	RDRAM STEP: Program timing parameters
	4E	RDRAM STEP: Power down exit
	4F	RDRAM STEP: Fast clock initialization
	50	RDRAM STEP: RDRAM core initialization
	51	RDRAM STEP: Levelization
	52	RDRAM STEP: Program power down configuration options
	53	RDRAM STEP: Begin normal operations - Page Policy and power management and IC bit
	54	RDRAM STEP: memory initialization complete - reenter MIT
	55	RDRAM STEP: Program power down configuration options
	56	RDRAM STEP: Begin normal ops - Page Policy, power management and set IC bit
	57	RDRAM STEP: Memory initialization complete - reenter MIT
03		Found quick start VM0 FMM object
	30	Seek relevant processor patch
	31	Apply processor patch
	32	Setup ICH GPIO base, SIO PME base, miscellaneous ICH settings
	33	Setup ICH GPIO attributes and values
	3A	Set ICH GPIO attributes and values
	3B	Set SIO GPIO attributes for GPIO10-17
	3C	Set SIO GPIO attributes for GPIO20-27
	3D	Set SIO GPIO attributes for GPIO30-37
	3E	Set SIO GPIO attributes for GPIO40-43
	3F	Set SIO GPIO attributes for GPIO50-57
	40	Set SIO GPIO attributes for GPIO60-61
	41	Set initial values for SIO GPIOs
	34	SMBUS initialization
	35	Initialize L1 cache for use as memory during memory initialization
04		Memory established
	60	Prepare for ECC scrubbing
	61	ECC scrubbing
	62	Restore context after ECC scrubbing
	63	Exit SMBUS
	64	ICH settings
	66	PIC
	68	SIO - Parallel port
	69	SIO - Serial port #1
	6A	SIO - Serial port #2 / DMA
	6B	SIO - Game port
	6C	SIO - MIDI
	6D	SIO - Exit configuration
	6E	Local APIC, FWH decode, runtime enable
05		Enable paging

Port 80	Port 81	Description
06		Unpack VM2
07		Transition to VM2
30		Interposer entry
	01	Interposer - Phase 0 - CMOS initialization
	02	Interposer - Phase 0 - IVT initialization
	03	Interposer - Phase 0 - Initialize compatibility table
	04	Interposer - Phase 0 - Runtime mouse fixes
	11	Interposer - Phase 1 - Reserved
	12	Interposer - Phase 1 - SCSI device numbering
	21	Interposer - Phase 2 - E820 data transfer
	22	Interposer - Phase 2 - Data repackaging
	23	Interposer - Phase 2 - Int 13h post
	24	Interposer - Phase 2 - Reserved
3A	31	Interposer - VM3 entry - Reserved
	32	Interposer - VM3 entry - Entering Int 19h
3F		DCC
40	XY	Scan for devices on PCI BUS where XY : X = Device(bits 7 - 3), Y = Bus(bits 2 - 0)
41		Route PCI IRQs to devices
42		Allocate memory resources to PCI devices
43		Allocate IO resources to PCI devices
44		Detect and shadow PCI Option ROM - Add in card
45		Detect and shadow PCI Option ROM - Embedded
4F		PCI Enumeration complete
50		SEL_FLASH_GetMaxRecSize had a severe parity error reading flash
70		Enumerate primary IDE channel
	02	Test for empty primary IDE channel
	03	Primary IDE channel discovery complete
	04	Primary IDE channel - check for ATAPI signature - master
	05	Primary IDE channel - master found - look for slave
	16	Primary IDE channel - ATAPI slave found
	26	Primary IDE channel - slave found
	36	Primary IDE channel - slave found
71		Enumerate secondary IDE channel
	82	Test for empty secondary IDE channel
	83	Secondary IDE channel discovery complete
	84	Secondary IDE channel - check for ATAPI signature - master
	85	Secondary IDE channel - master found - look for slave
	96	Secondary IDE channel - ATAPI slave found
	A6	Secondary IDE channel - slave found
	C6	Secondary IDE channel - slave found
72		Program IDE chipset settings
73		Program IDE devices
74		Setup IDE runtime data
75		Hard disk spin-up delay and Drive diagnostics
90		SIO initialization - Flex card detection
91		SIO initialization - serial
92		SIO initialization - parallel
93		SIO initialization - keyboard controller
94		SIO initialization - FDC

Port 80	Port 81	Description
95		Initialization - audio
A0		SMI handler - ACPI mode enable
A1		SMI handler - ACPI mode disable
A2		ACPI_LOAD_FACS
A3		ACPI_LOAD_FACD
A4		ACPI_LOAD_RSDT
A5		ACPI_LOAD_DSDT
A6		ACPI_LOAD_SSDT
A7		ACPI_LOAD_APIC
A8		TBD
A9		TBD
AA		TBD
AB		TBD
AC		ACPI_NO_CATALOG
AD		TBD
AE		ACPI_E820
AF		ACPI_FIXUPS
B8	00	AGP Pro Detected, prevent system from booting
B9	00	FMM initialization failed - Flash corruption - BIOS crisis recovery required
DE	AD	Double BIT ECC error detected (forced hang) - This code may be only temporary
F0		Enter BIOS recovery mode
F2		BIOS recovery - initialize flash
F4		BIOS recovery - enumerate PCI buses
F6		BIOS recovery - initialize floppy controller
F8		BIOS recovery - Extract BIOS update file from floppy
F9		BIOS recovery - Validate BIOS update contents
FA		BIOS recovery - Erase FWH blocks
FB		BIOS recovery - Enable FWH security
FC		BIOS recovery - Write buffer to FWH
FE		BIOS recovery - Operation successful
FF	F1	BIOS recovery - Flash initialization failure
	F2	BIOS recovery - Flash update operation failed
	F3	BIOS recovery - Read file from floppy operation failed
	F4	BIOS recovery - Flash erase operation failed
	F5	BIOS recovery - Flash write operation failed
	F6	BIOS recovery - File verify operation (checksum) failed
	F7	BIOS recovery/flash update - processor patch installation failed
	F8	BIOS recovery - File verify operation (invalid BIOS) failed
	F9	BIOS recovery - File verify operation (mismatched platform BIOS) failed
	FA	BIOS recovery - Boot block incompatible with BIOS
	FB	BIOS recovery - Flash verify after write failed

LANDMARK

Same as BIOSYS BIOS. Beeps as for IBM AT. Codes sent to ports 280 and 80.

XT Jumpstart

Code	Meaning	Code	Meaning
01	Jump to reset area in ROM BIOS	16	Setup and init cassette function
02	Initialize DMA page register	17	Setup and init bootstrap function
03	Initialize DMA refresh register	18	Setup and init keyboard function
04	Clear all RAM	19	Enable speaker
05	Perform RAM test on 1st 64k	1A	Setup timer 0 for the real time clock
06	Clear 1st 64k	1B	Enable RTC
07	Initialize BIOS stack to 0:FC0	1C	Setup timer 2 for the beeper
08	Set the equipment flag based on switches	1D	Size memory: write 55AA/AA55 to 1st/last word in segment
09	Initialize default interrupt vectors	1E	Read 1st and last word of segment
0A	Initialize 8255 if it exists and enable parity	1F	Compare 1st and last words
0B	Initialize 8259 and enable interrupts	20	Report determined memory size to screen
0C	Setup adapters and peripherals	21	Perform checksum on ROM BIOS
0D	Setup video	22	If cold boot perform complete RAM testing
0E	Initialize video	23	Move system stack to bottom of memory and save pointer at 40:0E
0F	Initialize equipment	24	Reset parity after RAM sizing
10	Initialize memory configuration in RAM (currently = 64K)	25	Enable timer and keyboard interrupts
11	Setup timer function	26	Setup the serial and parallel ports
12	Initialize timer function	27	Setup the game port
13	Setup time of day function	28	Setup the floppy disk controller
14	Initialize time of day function	29	Scan for optional ROM in 2K chunks from C8000 to start of BIOS
15	Setup and init print screen function	2A	Boot System

AT Jumpstart

Code	Meaning	Code	Meaning
03	1 short beep when first awake	32	Size memory by testing it
04	Initialize bell tone	33	Adjust memory configuration
05	Enable CMOS RAM	33	Verify CMOS RAM size
06	Reset video controller	34	Enable I/O parity
07	Disable I/O parity	35	Test 8259
08	Start memory refresh	36	Bytes swap test
09	Clear reset flag in RAM	37	Test NMI
0A	Test DMA page registers	38	Timer test
10	Use CMOS to determine if soft reset	39	Initialize timer A
11	Perform ROM checksum	3A	Protected mode memory test
12	Test timer A	3B	Test keyboard
13	Test DMA channel A	3C	Test keyboard interrupt
14	Test DMA channel B	3D	Enable A20
15	Test refresh	3E	Reset hard disk controller

Code	Meaning	Code	Meaning
16	Flush 8042 input buffer	3F	Setup floppy controller
17	Reset 8042	40	Test floppies
18	Get keyboard switch	41	Setup keyboard (NumLock)
19	Initialise keyboard	42	Enable timer interrupt
1A	Clear any existing parity	43	Check for dual floppy/hard disk controller
1B	Enable on-board parity	44	Find floppy drive A type
1C	Test base 64K memory	45	Find floppy drive B type
1D	Test base 64k parity	46	Reset hard disk
1E	Initialize POST stack	47	Enable slave DMA
20	Put keyboard # in RAM	63	Set video interrupt vector
65	Set video speed	48	Call any external ROMs
21	Test protected mode registers	49	Initialize printer
22	Initialize 8259 interrupts	4A	Initialize serial
23	Zero all 256 interrupts	4B	Initialize 80287
24	Initialize interrupts 0-1fh	4C	Read CMOS RAM status
25	Perform DRAM checksum	4D	Check CMOS configuration against hardware found
26	Adjust configuration based on hardware	70	Check CMOS against memory found
27	Check manu switch (may exit POST)	4E	Initialize timer ticks
28	Initialize video controller	4F	Enable IRQ9
2A	Test video memory	50	Enable on-board parity
2B	Test video sync	51	Call add-on card ROM
2C	Look for external video	52	Enable keyboard interrupt
2D	Change video configuration if external video	53	Reset printer
2E	Unused	60	Check for any errors
2F	Initialize video controller	61	One short beep
30	Change video interrupt	62	Print sign-on message
31	Print any POST messages	64	Perform boot

MAGNAVOX

See Philips.

MICRONICS

Makes its own upgrades for Phoenix.

MR BIOS

The last code emitted is the one that failed. There may also be a message on screen. Beep codes are in a binary format and are preceded by a high and low tone (described elsewhere). Check also Nasty Noises for more codes.

POST Procedures

Procedure	Meaning
Reset	See if a warm boot (Ctrl+Alt+Del) or a cold boot (Reset) is needed.
Chipset Initialisation	Reset the support chips (8259) DMAs and timers to defaults before proceeding.
Disable Chips	Disable NMI/DMA and Video (6845) for accurate results later. Failure here normally a NMI generated by one of the disabled chips.
ROM BIOS Checksum	Perform checksum test, add a preset value stored in BIOS to create value of 00.
DMA Test	Perform a test of the page registers in the DMA controller.
Keyboard Controller Test	Send a command to the 8042 keyboard controller to perform a selftest. The keyboard controller will return a buffer and error buffer address.
Chipset Initialisation	Initialise the DMA (8237)/PIC (8259)/PIT (8254) and RTC chips.
DMA Test	Test the registers of the master 16-bit and slave 8-bit DMA controllers by writing bit patterns and reading the results.
Cache/Shadow Disable	Disable cache and shadow RAM before processing with POST.
Refresh	Test interval in which PIT (8254) chip sends a refresh signal to the DMA chips.
Base 64K Memory	Test the first 64K of system memory with a walking-bit pattern.
PIC Test	Test the mask registers of the master and slave interrupt controllers by setting the mask-bit in the registers and generating an interrupt to see if the interrupt is trapped. Then test the additional registers in the PICs with a walking-bit pattern.
PIT Test	Test interrupt timer channels 0-2 and initialise if no failures occur.
RTC	Perform read/write test of RTC portion of CMOS and initialise if no failures occur.
Video	Test and initialise the video adapter, which will perform an internal diagnostic and sign on before returning an OK status.
CMOS Checksum	Perform a checksum on the system RAM.
Keybd Initialisation	Initialise the keyboard and read the buffer address for errors.

OEM Specific

Procedure	Meaning
Base Memory Test	Test memory addresses between 64-640K with a walking-bit pattern. There may be a hex display of the failing it.
Keyboard 2nd Init	Tries again if the first failed.
Protected Mode Test	Test the ability of the keyboard controller address line 20 to respond to commands that switch the CPU in and out of protected mode.
Extended Memory	Test addresses above 1 Mb in 64K blocks and perform pattern tests.
OEM Memory	Normally test the cache controller and shadow RAM.
RTC Time Test	Test the write active line of the RTC/CMOS chip. Check bad CMOS/battery
Serial Port	Generate an interrupt of the CPU through I/O ports reserved for RS232 devices. Failure to see a device could be the device itself or more than one set to the same port. Checks are only made for two devices.
Parallel	Check for parallel devices. Failure to see a device could be the device itself or more than one using the same port. Checks are only made for three.
NPU Test	Perform a register test on the NPU then initialise if passed.
Floppy Test	Test floppy controller and drive.

Procedure	Meaning
Fixed Disk	Test fixed disk controller and drive and compare the results against CMOS. This is skipped if no drive is installed.
CMOS Update	Update information in CMOS RAM based on the previous results.

Non-Fatal Errors

Procedure	Meaning
Lock Check	Check if a system lock-byte is set and wait for user response if an error is generated. Check the panel lock or circuitry.
NumLock/Pwd/Setup	Set NumLock on (if set) and ask for password (if set) and display setup message.
Typematic Rate	Set the typematic rate.
Floppy Disk	Perform any further initialisation needed.
Hard Disk	Perform any further initialisation needed.
Video Mode	Set primary video mode and display any errors found during initialisation routines.
Shadow/Cache Enable	
Adapter ROM	Initialise adapters with a ROM signature of 55AA. Self tests will be performed by the equipment concerned before handing back control to the POST.
Video Monitor Mode	Set the video mode based on the information in the CMOS and update the time variables from the RTC.
Parity/NMI Enable	Enable NMI by setting bit 7 of CMOS address 41 and enable parity.
Set Stack	Set last significant byte of stack pointer and install shadow RAM at E000 if in CMOS.
Acknowledge	Acknowledge errors and set primary video mode before calling Int 19 boot loader. Errors reported will await a keyboard response before proceeding. Errors beyond this point are normally software related.

3.3

Code	Meaning
00	Cold-Boot commences (Not seen with warm-boot).
01	HOOK 00 OEM specific typically resets chipset to default
02	Disable critical I/O: 6845s CRT; 8237s DMA; 7675 floppy and parity latches
03	BIOS checksum test
04	DMA Page register test (Ports 81-8F)
05	8042 (Keyboard Controller) Self test.
06	Game Port init: 8237 master/slave; 8254 ch2/1; RTC Reg3 F/A; 8259 master/slave
07	HOOK 01. OEM specific; typically disables cache/shadow
08	Refresh toggle test (PORTB)
09	Pattern test master/slave 8237s; eight 16-bit regs each
0A	Base 64K memory test
0B	Pattern test master/slave 8259 mask regs
0C	8259/IRQ tests purge powerup ints
0D	8254 channel-0 test and initialization
0E	8254 channel-2 toggle test speaker circuitry
0F	RTC tests/inits: Init REG-B; write/readback NVRAM. PIE test
10	Video Initialization.
11	CMOS Checksum test
12	Sign-on msg. Accept KB BAT; perform 1st try KB unit; cold boot delay
13	HOOK 02. OEM specific; select 8MHz bus
14	Size/Test base memory (low 64K already done)

Code	Meaning
15	Perform 2nd try KB init if necessary
16	HOOK 03. OEM specific. Size/Test cache
17	Test A20 gate off; then on.
18	Size/Test extended memory
19	HOOK 04 and Size/Test system memory (special OEM memory)
1A	Test RTC Update-In-Progress and validate time
1B	Serial port determination off-board/on-board
1C	Parallel port determination off-board/on-board
1D	Copro determination/initialization
1E	Floppy controller test/determination CMOS validation
1F	Fixed Disk controller test/determination CMOS validation
20	Rigorous CMOS parameter validation, display other config changes
21	Front-Panel lock check; wait for user to acknowledge errors
22	Set NumLock; Password-Security Trap; despatch to setup utility
23	HOOK 05. OEM specific.
24	Set typematic rate. 28 HOOK 6. OEM specific, typically enables shadow, cache, turbo
25	Floppy subsystem initialization
26	Fixed subsystem initialization
27	ACK errors; set primary adapter video mode
29	Disable A20-gate; set low stack, install C800, E000 ROMs.
2A	ACK errors; set video mode, set DOS time variables from RTC.
2B	Enable parity checking and NMI
2C	Set low stack, Install E000 ROM
2D	ACK errors, set primary video mode.
2E	HOOK 07. OEM specific. Log-in EMS (if built-in).
2F	Pass control to INT 19.

3.4

Code	Meaning
00	Cold Start. Output EDX register to I/O ports 85h, 86h, 8Dh, 8Eh for later use
01	Init Custom KBD controller, disable CPU cache, cold init onboard I/O chipset, size & test RAM & cache
02	Disable critical I/O: 6845s CRT; 8237s DMA; 7675 floppy and parity latches (monitor, DMA, FDC, I/O ports, Speaker, NMI).
03	BIOS checksum test
04	DMA Page register test (Ports 81-8F)
05	8042 (Keyboard Controller) Self test. Enable A20 Gate.
06	Init ISA I/O
07	Warm initialize custom KBD controller, warm initialize onboard I/O chipset.
08	Refresh toggle test (PORTB)
09	Pattern test master/slave 8237s
0A	Base 64K memory test. Test Master 8259 mask, test Slave 8259 mask
0B	Pattern test master/slave 8259 mask
0C	Test 8259 Slave, test 8259 slave's interrupt range, initialize interrupt vectors 00-77h, init KBD buffer variables.
0D	8254 channel-0 test
0E	8254 channel-2
0F	RTC test, CMOS RAM r/w test
10	Turn on monitor, show possible error messages.

Code	Meaning
11	CMOS Checksum test
12	Call video ROM init routine. Sign-on msg.
13	Set 8MHz AT bus
14	Size/Test base memory, Stuck NMI
15	No KB and power on: Perform 2nd try KB init if necessary
16	Size/Test cache
17	Test A20 gate off; then on.
18	Size/Test external memory, Stuck NMI
19	Size/Test system memory, Stuck NMI
1A	Test RTC time
1B	Serial port determination off-board/on-board
1C	Parallel port determination off-board/on-board
1D	Copro initialization
1E	Floppy controller determination
1F	IDE determination
20	Display CMOS config changes
21	Clear Screens
22	Set NumLock LED; perform security functions
23	Final determination of onboard Serial/Parallel ports.
24	Set typematic rate
25	Floppy subsystem initialization
26	ATA disks initialization
27	Set primary adapter video mode
28	WB-CPU support, Green PC: purge 8259 slave, relieve trapped IRRs before enabling PwrMgmt, set 8042 pins, Ctrl-Alt-Del possible, Enable CPU Features.
29	Disable A20-gate; install C800, E000 ROMs.
2A	Clear primary screen, convert RTC to system ticks, set final DOS timer variables.
2B	Enable NMI and latch
2C	Reserved
2D	Reserved.
2E	Fast A20: Fix A20.
2F	Purge 8259 slave; relieve any trapped IRRs before enabling Green-PC. Pass control to INT 19.
32	Test CPU Burst
33	Reserved
34	Determine 8042, Set 8042 Warm-Boot flag STS.2
35	Test HMA Wrap, Verify A20 enabled via F000:10 HMA
36	Reserved
37	Validate CPU: CPU Step NZ, CPUID Check. Disable CPU features
38	Set 8042 pins (Hi-Speed, Cache-off)
39	PCI Bus: Load PCI; Processor Vector init'd, BIOS Vector init'd, OEM Vector init'd
3A	Scan PCI Bus
3B	Initialize PCI Bus with intermediate defaults
3C	Initialize PCI OEM with intermediate defaults, OEM bridge
3D	PCI Bus or PLUGnPLAY: Initialize AT Slotmap from AT-Bus CDE usage
3E	Find phantom CDE ROM PCI-cards
3F	PCI Bus: final Fast-Back-to-Back state
40	OEM POST Initialization, Hook Audio
41	Allocate I/O on PCI-Bus, logs-in PCI-IDE
42	Hook PCI-ATA chips

Code	Meaning
43	Allocate IRQs on the PCI Bus
44	Allocate/enable PCI Memory/ROM space
45	Determine PS/2 Mouse
46	Map IRQs to PCI Bus per user CMOS, Enable ATA IRQs.
47	PCI-ROM install, note user CMOS
48	IfSetup conditions: execute setup utility
49	Test F000 Shadow integrity, Transfer EPROM to Shadow-RAM
4A	Hook VL ATA Chip
4B	Identify and spin-up all drives
4C	Detect Sec IRQ, if VL/AT-Bus IDE exists but its IRQ not known yet, then autodetect it
4D	Detect/log 32-bit I/O ATA devices
4E	ATAPI drive M/S bitmap to Shadow-RAM, Set INT13 Vector
4F	Finalize Shadow-RAM variables
50	Chain INT 13
51	Load PnP, Processor Vector init'd, BIOS Vector init'd, OEM Vector init'd
52	Scan PLUGnPLAY, update PnP Device Count
53	Supplement IRQ usage-AT IRQs
54	Conditionally assign everything PnP wants
58	Perform OEM Custom boot sequence just prior to INT 19 boot
59	Return from OEM custom boot sequence. Pass control to 1NT 19 boot
5A	Display MR BIOS logo
88	Dead motherboard and/or CPU and/or BIOS ROM.
FF	BIOS POST Finished.

Msg	Low-High	Problem
03	LH-LLL	ROM-BIOS Checksum Failure
04	LH-HLL	DMA Page Register Failure
05	LH-LHL	Keyboard Controller Selftest Failure
08	LH-HHL	Memory Refresh Circuitry Failure
09	LH-LLH	Master (16 bit) DMA Controller Failure
09	LH-HLH	Slave (8 bit) DMA Controller Failure
0A	LH-LLLL	Base 64K Pattern Test Failure
0A	LH-HLLL	Base 64K Parity Circuitry Failure
0A	LH-LHLL	Base 64K Parity Error
0A	LH-HHLL	Base 64K Data Bus Failure
0A	LH-LLHL	Base 64K Address Bus Failure
0A	LH-HLHL	Base 64K Block Access Read Failure
0A	LH-LHHL	Base 64K Block Access Read/Write Failure
0B	LH-HHHL	Master 8259 (Port 21) Failure
0B	LH-LLLH	Slave 8259 (Port A1) Failure
0C	LH-HLLH	Master 8259 (Port 20) Interrupt Address Error
0C	LH-LHLH	Slave 8259 (Port A0) Interrupt Address Error
0C	LH-HHLH	8259 (Port 20/A0) Interrupt Address Error
0C	LH-LLHH	Master 8259 (Port 20) Stuck Interrupt Error
0C	LH-HLHH	Slave 8259 (Port A0) Stuck Interrupt Error
0C	LH-LHHH	System Timer 8254 CH0 / IRQ0 Interrupt Failure
0D	LH-HHHH	8254 Channel 0 (System Timer) Failure
0E	LH-LLLLH	8254 Channel 2 (Speaker) Failure

Msg	Low-High	Problem
0E	LH-HLLLH	8254 OUT2 (Speaker Detect) Failure
0F	LH-LHLLH	CMOS RAM Read/Write Test Failure
0F	LH-HHLLH	RTC Periodic Interrupt / IRQ8 Failure
10	LH-LLHLH	Video ROM Checksum Failure at Address XXXX Mono Card Memory Error at Address XXXX Mono Card Memory Address Line Error at XXXX CGA Card Memory Error at Address XXXX CGA Card Address Line Error at Address XXXX
11	(None)	Real Time Clock (RTC) Battery is Discharged
11	(None)	Battery Backed Memory (CMOS) is Corrupt
12	LH-HLHLH	Keyboard Controller Failure
14/18/19	LH-LHHLH	Memory Parity Error
14/18/19	LH-HHHLH	I/O Channel Error
14		
18		
19	(None)	RAM Pattern Test Failed at XXXX Parity Circuit Failure in Bank XXXX Data Bus Test Failed: Address XXXX Address Line Test Failed at XXXX Block Access Read Failure at Address XXXX Block Access Read/Write Failure: Address XXXX Banks Decode to Same Location: XXXX and YYYY
15	(None)	Keyboard Error-Stuck KeyKeyboard Failure or no Keyboard Present
17	LH-LLLHH	A20 Test Failure Due to 8042 Timeout
17	LH-HLLHH	A20 Gate Stuck in Disabled State (A20=0)
17	(None)	A20 Gate Stuck in Asserted State (A20 Follows CPU)
1A	LH-LHLHH	Real Time Clock (RTC) is Not Updating
1A	(None)	Real Time Clock (RTC) Settings are Invalid
1E	(None)	Diskette CMOS Configuration is Invalid Diskette Controller Failure Diskette Drive A: Failure Diskette Drive B: Failure
1F	(None)	Fixed Disk CMOS Configuration is Invalid Fixed Disk C: (80) Failure Fixed Disk D: (81) Failure Please Wait for Fixed Disk to Spin Up
20	(None)	Fixed Disk Configuration Change Diskette Configuration Change Serial Port Configuration Change Parallel Port Configuration Change Video Configuration Change Memory Configuration Change Numeric Coprocessor Configuration Change
21	(None)	System Key in Locked Position-Turn Key to Unlocked Posn
29	(None)	Adapter ROM Checksum Failure at Address XXXX

MYLEX/EUROSOFT

Derived from Eurosoft BIOS, mainly for Mylex EISA boards.

4.71

Pass	Fail	Meaning
03	04	DMA page registers test
05	06	Keyboard reply test
07	08	Keyboard self-test
09	0A	8042 keyboard controller able to read links
0B		RATMOD/DIAG link
0C	0D	Keyboard acceptance of 60H
0E	0F	Keyboard acceptance of parameter
10	11	Read keyboard command byte
12	13	Keyboard command byte came back
14	15	RAM refresh toggle test
16	17	RAM bit test
18	19	RAM parity test
1A	1B	CMOS RAM test
1C	1D	CMOS RAM battery test
1E	1F	CMOS RAM checksum test
	20	CMOS RAM battery fault bit set
21	22	Master DMA controller test
21	23	Slave DMA controller 2 test
24		Protected mode entered safely
25		RAM test completed
26	27	BIOS ROM checksum test
28		Protected mode exit
29	2A	Keyboard power-up reply received test
2B	2C	Keyboard disable command acceptance test
	2D	Video display presence check
	2E	POST Errors were reported
	2F	About to halt
30		Protected mode entered safely (2)
31		RAM test complete
33		Master interrupt controller test
34	35	Slave interrupt controller test
36	37	Chipset initialization
38	39	System BIOS shadowed
3A	3B	Video BIOS shadowed

EISA/ISA

Code	Meaning	Code	
01	Processor test	16	Initialise output port of keyboard controller
02	DMA Page Register	17	Keyboard interrupt test
03	8042 keyboard controller	18	Initialise keyboard
04	BIOS ROM Checksum error	19	RTC clock test failure

Code	Meaning	Code	
05	Send keyboard command test bad	1A	Maths copro test failure
06	CMOS RAM Test	1B	Reset hard/floppy controller
07	RAM Refresh Test	1C	Initialise floppy drive
08	1st 64K memory test	1D	Initialise hard drive
09	8237 DMA controller test	1E	Initialise ROMs in C000-DFFF
0A	Initialise DMA controller	1F	Initialise serial and parallel ports
0B	Interrupt Test	20	Initialise time of day in RTC
0C	Determine RAM size	21	Initialise ROMs in E000-EFFF
0D	Initialise video	22	Look for boot device
0E	EGA/VGA ROM checksum test failed	23	Boot from floppy disk
10	Search for monochrome card	24	Boot from hard disk
11	Search for colour card	25	Gate A20 enable/disable failure
12	Word splitter and byte shifter test failed	26	Parity error occurred
13	Keyboard Test	30	DDNIL bit scan failure
14	RAM Test failed	FF	Fatal error occurred and system halted
15	Timer test error		

NCR

Purchased 1991 by AT&T. See AMI pre-0490 for PC386, others below. NCR ones use LPT1.

Architecture	Typical PC	BIOS	POST Code Port
XT	PC6	NCR	378 or 3BC (LPT 1)
AT (ISA)	3728, 3204, PC 916	NCR	80 and 378 or 3BC (LPT 1)
	PC386	AMI Pre-0490	80
Micro Channel	3421	Phoenix	680 and 3BC

PC6

Code	Meanings
AA	8088 CPU failure
B1	2764 EPROM checksum failure
B2	8237 DMA controller failure
B3	8253 timer failure
B4	RAM failure. Halts if error in first 64K, otherwise displays MEMORY ERROR.
B5	8259 interrupt controller failure. Displays INTERRUPT FAILURE
B6	RAM parity error. Displays ERROR IN BASE MEMORY or ERROR ON EXPANSION CARD.
BB	All tests passed

3302/3304/3728/PC916SX

Code	Meaning
01	Test CPU registers
02	Test system I/0 port-write and read port 61 to confirm will handle RAM refresh.
03	Test ROM BIOS checksum
04	Test DMA page registers

Code	Meaning
05	Test timer channel 1 (refresh)
06	Test timer channel 2 (speaker)
07	Test RAM refresh logic. Also verifies timer is working.
08	Test base 64K RAM
09	Test 8/16 bit bus conversion
0A	Test interrupt controller 1
0B	Test interrupt controller 2
0C	Test I/O controller
0D	Test CMOS RAM read/write
0E	Test for battery power low or interrupted since last test
0F	Test CMOS RAM checksum
10	Test CPU protected mode
11	Test video configuration in CMOS RAM or display switch
12	Test primary video controller
13	Test secondary video controller
20	Display results of tests to this point
21	Test DMA controller 1
22	Test DMA controller 2
23	Test Timer channel 0 (system timer tick)
24	Initialize interrupt controllers
25	Test interrupts
26	Test interrupts
30	Check base 640K memory size
31	Check extended memory size
32	Test higher 8 address lines
33	Test base memory
34	Test extended memory
40	Test keyboard-enable/disable
41	Test keyboard-reset
42	Test keyboard-clock low
43	Test keyboard-for interrupt, enable keyboard, init pointers, write out subcommand
44	Test 8086 address overrun compatibility (gate A20)
50	Set up hardware interrupt vectors
51	Enable interrupt from timer channel 0
52	Security ROM
60	Test floppy disk controller and drive
61	Test hard disk controller
62	Initialize floppy drives
63	Initialize hard drives
70	Test real time clock
71	Set time of day in real time clock
72	Check parallel interfaces
73	Check serial interfaces
74	Check for and execute adapter option ROMs
75	Check if math coprocessor is installed and enable interrupt
76	Enable keyboard and real time clock interrupts
F0	System not configured correctly, or hardware defect
F1	Scan for and execute motherboard option ROMs
F2	INT 19 to boot operating system-No POST errors.

PC916 5/6

*halt on error if loop jumper installed in keyboard connector

Code	Meaning
01	Test CPU registers, reset video cards, display diagnostic messages
02	Verify port 61, disable non-maskable interrupt, start speaker timer channel 2
03	Test ROM BIOS checksum
04	Test DMA page registers
05	Test timer channel 1 (refresh)
06	Test timer channel 2 (speaker)
07	Test refresh logic by reading port 61 bit 4 every 15 microseconds
08	Test base 64K RAM
09	Test 8/16-bit bus converting logic, initialize both interrupt controllers
0A	Test interrupt mask register A
0B	Test interrupt mask register B, write temporary interrupt vector table for INT 00-77
0C	Test 8042/8742 keyboard controller
0D	Test CMOS RAM shutdown byte
0E*	Test CMOS RAM battery power low or interrupted since last test
0F*	Test CMOS RAM checksum; initialize periodic rate
10	Test CPU protected mode
11	Test video configuration in CMOS RAM or display switch, look for advanced video card ROM in segment C000, initialize interrupt vectors.
12	Initialize and test primary video controller
13	Primary video error, test secondary video controller
14	Test disabling Speed stretch enable/disable port 69 bit 0=1
15	Start refresh timer 1 counter 1, disable speed switch timer 2, counter 2
16	Enable then disable speed stretch enable/disable port 69 bit 0
17	Clear write protect bit
18	Write/verify global/local/interrupt descriptor table registers; copy ROM BIOS to shadow RAM F000
19	Verify RAM to ROM BIOS copy OK; reinitialize restart vector, check and execute for burn-in ROM D000. Disable real time clock in CMOS status reg B, reset and initialize video cards.
IA	Command 8042 to execute self-test and verify result
1B	Test 64K Shadow RAM in segment F000
20	Display results of tests to this point
21	Test DMA controller 1
22	Test DMA controller 2 and initialize all 8 channels
23	Test timer 1 counter 0 840 ns clock timer for IRQ0 (INT8)
24	Initialize both interrupt controllers
25	Check for unexpected (hot) interrupts
26	Wait for interrupt
27*	Test timer 2 counter 0 for NMI (INT02), failsafe
28*	Test timer 2 counter 1 (INT72-74)
30	Check base 640K memory size
31	Check extended memory size (max 256M RAM on 5.2, 6 BIOS)
32	Test higher 8 address lines for mirror addresses (5.x BIOS)
33*	Test base memory
34*	Test extended memory (up to 256M)
35*	Test RAM in E000 (v6 BIOS-also test keyboard shutdown command FE-shutdown path 0B)
40	Test keyboard-enable/disable
41	Test keyboard-reset command FF (halt on error if loop jumper not installed)

Code	Meaning
42	Test keyboard-clock low (halt on err if loop jumper not installed)
43	Test keyboard-check for interrupt, enable keyboard, initialize buffer pointers, verify keyboard unlocked, disable external interrupts mask A=F, turn on write protect for RAM E000-FFFF, write out subcommand (halt on error if loop jumper not installed).
44	Test address overrun compatibility (turn off gate A20, 8042 P2 bit 1 = 0)
45	v6 BIOS-Init mouse, en IRQ1 (INT09)keyboard (15 IRQs, 1 disabled), disp Press F1 for Setup.
50	Set up hardware interrupt vectors 0-15, 70-77
51	Enable IRQ0 interval interrupt 08 from timer channel 0; enable ext interrupts (STI)
60	Test for floppy/hard disk controller and drive
61	Test cylinder register for disk controller
62	Initialize floppy drives
63	Initialize hard drives
70*	Test real time clock
71	Set interval timer RAM counts
72	Configure and test parallel interfaces
73	Configure and test serial interfaces
74	Check for and execute adapter option ROMs C8000-DFFFF
75*	Test math coprocessor if installed, and enable interrupt
76	Enable keyboard and real time clock IRQ8 (INT 70) interrupts; enable slave interrupt controller 2 via PIC 1 mask bit 2=0.
F0	Display logged errors. Halt if locked; loop if loop jumper installed
F1	Test system code at segment E000 (v5.x BIOS only); v6 BIOS-copy video ROM BIOS (if present) to shadow RAM if system ROM is absent and switch pack switch 1 is on
F2	INT 19 to boot operating system-No POST errors
F3	Go to setup if F1 key pressed. v6 BIOS: execute floppy diagnostic if Ctrl-D pressed, enable failsafe NMI port 61 bit 2=0, enable parity error port 61 bit 3=0, enable NMI.
F4	v5.x BIOS only-Display speed setting
F4	v6 BIOS-Display speed setting Auto, high, fixed
F5	v5.x BIOS only-initialize counter 2 for speed requested
F6	v5.x BIOS only-Test base memory (long test in 5.2 BIOS)
F6	v6 BIOS only-Test base memory (long test) if F2 pressed
F7	v5.x BIOS only-Test extended memory (long test in 5.2 BIOS)
F7	v6 BIOS only-Long test extended memory if F2 pressed

OLIVETTI

For EISA and PS/2, code is issued after the test has passed, so a stuck code indicates the next test failed. Codes are sent to printer ports 3BC (mono adapter's parallel port), 278, or 378; they will not be printed as no strobe is sent. AT&Ts using the Olivetti motherboard and BIOS (e.g. the AT&T 6300) do the same.

1076/AT&T 6312/WGS 80286

The first checkpoint, 40, resets and initializes a test monitoring device on the parallel port. When an error occurs, the most recent checkpoint code sent to 378 is exclusive-ored with 3F to complement the lower 6 bits, and then sent to 378, so if the refresh test fails (45), the POST card will show 7B because the most recent code sent before the failure was 44. If an error occurs, the POST tries to run through activities that display a message on the monitor, showing tttt Error: xx, where tttt is the name of the

failing routine, and xx is a suberror number. If the error is fatal, the display will show *Unrecoverable Power-Up Error*, wait for F1 to be pressed, and return to failing test. If video has failed, there are beep codes.

Pass	Fail	Meaning
40		Dummy check-reset black box
41	7F	80286 CPU flags and register test
42	7E	Check and verify shutdown code-read keyboard status from port 64. if shutdown bit is set, read shutdown byte from CMOS (and clear location there), check for illegal shutdown condition, initialize the 8259s unless shutdown is 9 or A, and jump to the correct routine to handle the shutdown: 0= warm boot (go to next test), 1= return to advanced protected mode test, 2= return to memory test above 1 Mb, 3=return to protected mode test 2, 4=INT19, 5=send EOI to 8259 and return to user routine, 9=int15 block move, A=return to user routine.
43	7D	Checksum test the BIOS ROMs-verify contents add up to 0.
44	7C	Test the 8253 timer-check all 3 timers for not counting, counting too slowly, or counting too fast. Suberror display is the bad timer number 0, 1, or 2.
45	7B	Start memory refresh and verify it occurs every 15.1 microseconds. Init the manufacturing test byte in RAM.
46	7A	Command the 8041 keyboard controller to do a self-test. Suberror display is 1 if error return, 2 if self-test times out.
47	79	Test the first 8K of RAM in 4 passes: 1) write into each word a data value corresponding to the address; 2) invert all bits written; 3) write an odd parity pattern; 4) write zeros. Only pass 4 is done on a warm boot. Beep once when this test passes. Install dummy interrupt vectors, set up the stack and other memory areas. display power-on banner on screen.
48	78	Test 80286 in protected mode 1-pattern test all IDT and GDT registers, verify LIDT, SIDT, LGDT, and SGDT instructions.
49	77	Test CMOS RAM shutdown byte with a pattern, then clear it.
4A	76	Test 80286 in protected mode 2-put CPU into protected mode, check it's there, then return to real mode
4B	75	Test RAM from 8K to 640K (cold boot only)-display progress for each 128K block; write, read, and compare the address and inverted address into each word.
4C	74	Test RAM above 1 Mb - same as below 1 Mb test. Also verify CPU runs properly in prot mode.
4D	73	Test for NMI-installs NMI vector in interrupt table and small service routine. Disables I/O and memory parity errors, then checks for hot NMI.
4E	72	Test for RAM parity-turn NMI parity checking back on, and run a pattern test on the parity checking circuit, monitoring for a parity error.
50	71	Test 8259 interrupt controller 1-pattern test the mask register, install interrupt vectors for IRQs, mask them all off. look for hot interrupt coming through mask, set timer 0 to issue an interrupt, unmask it, count down, and expect the interrupt. Suberror display is l=no in, 2=timer doesn't count, 3=int occurred when masked, 4=bad mask register.
51	6F	Test 8259 interrupt controller 2-same as # 1, but no timer test is done. Suberror display is 5=int occurs wen masked, 6=bad mask register. When the test passes, install the interrupt service routine pointer in the vector table, mask off all interrupts. and display PASS message.
52	6E	Test DMA page register-marching bit test on all page registers.
53	6D	Test 8237 DMA controller 1-pattern test all read/write registers. Initialize each channel into the correct mode for BIOS. Suberror 1 display if failure.
54	6C	Test 8237 DMA controller 2-pattern test all read/write registers. Initialize each channel into the correct mode for BIOS. Suberror 3 display if failure.
55	6B	Test PIC port-write/read pattern test speaker port 61.
56	6A	Test keyboard controller-reset the keyboard and initiate self-test Suberror display is l=bad keyboard self-test completion code. 2=stuck key. 3=no keyboard interrupt Otherwise, display pass message, and set up keyboard id flags and buffer in BIOS RAM area.
57	69	Test CMOS clock/calendar chip-verify accurate time keeping and display pass message.
59	68	Test 80286 advanced protected mode-tests LDT, SDT, LTR, STR, VERR, VERW, LAR, SLR, ARPL instructions; forces exception ints 13 and 5. Suberror display is 3=instruction error, 4=no exception or protection violation. Otherwise display prot mode pass message.

Pass	Fail	Meaning
5A	66	Test CMOS RAM battery and display message if low.
5B	65	Test CMOS RAM non-destructively-copy contents to base memory, write/read pattern test CMOS RAM, restore contents. Suberror 2 if failure.
5C	64	Verify CMOS RAM checksum.
5D	63	Test parallel port by writing AA to 3BC, 278 and 378, and set config info in BIOS RAM.
5E	62	Test serial port configuration-read 3FA and 3FA and assume a UART is present if values not FF. Set up port addresses and timeout values in BIOS RAM area.
5F	61	Test configuration of memory below 640K-compare memory size stored in CMOS RAM with result of earlier test. Display message to run setup if different.
60	60	Test configuration of memory above 1M-compare memory size stored in CMOS RAM with result of earlier test. Display message to run setup if different.
61	5F	Test configuration of 80287 math coprocessor chip -verify math chip same as in CMOS RAM info. Display pass or run setup message.
62	5E	Test configuration of game port at 201 and set equipment bit in BIOS RAM data area.
62	5D	Test keylock switch and wait till unlocked.
63	5D	Test hard drive configuration-initialize controller and drive. Display whether drives are present, and message to run setup if not same as CMOS RAM info.
64	5C	Configure floppy drives A and B-initialize controller and drive. Display whether drives are present, and message to run setup if not same as CMOS RAM info.
66	5B	Test option ROMs-look for signature AA5 each 2K beginning at C8000, run checksum and display error if it occurs. Otherwise pass control to the ROM so it can initialize, and display pass message when done.
		INT 19-boot the system.

M20

Not a true IBM clone, as it had a Zilog Z8001 CPU. Also, a typical POST card will not fit in a slot, so you can only monitor codes from the parallel port. The POST shows a triangle, diamond, or 4 lines on the screen to indicate early POST failure, as shown in the table.

Code	Meaning
	Program video controller using load, output, and jump relative instructions (need video).
Triangle	Test Z8001 CPU registers and instructions; infinite loop if failure.
Triangle	Test RAM module; infinite loop if failure; also send msg to printer: E Mc bb ssss wwww. c = RAM configuration # (3 = 1 32K memory card); bb = hex 16K bank # (0,4,5,6,9,A=motherboard; 1,7,B=expansion board 1; 2=expansion board 2; 3,11,12=cxpansion board 3); ssss = what data should be; wwww = what data was (hx).
4 vertical lines	Test CPU call and trap instructions; infinite loop if failure.
Diamond	Initialize screen and printer drivers.
	Program UARTs (serial chips) and 8253 baud rate generator for keyboard at 1200 baud and RS232 at 9600. Now test remaining circuits and send codes to display and printer.
EC0	8255 parallel interface chip test failed
EC1	6845 CRT controller chip test failed
EC2	1797 floppy disk controller chip test failed
EC3	8253 timer chip test failed
EC4	8251 keyboard serial interface chip test failed
EC5	8251 RS232 serial interface chip test failed
EC6	8259 interrupt controller chip test failed
EK0	Keyboard did not respond
EK1	Keyboard responded, but self-test failed
ED1	Disk drive 1 test failed
ED0	Disk drive 0 test failed

Code	Meaning
E10	Non-vectored interrupt error
E11	Vectored interrupt error

M21/M24 (AT&T 6300)

The M24 went to the US as the AT&T 6300. It had an 8086, so was faster than the PC, albeit difficult to work on. codes are sent to 378 (LPT1). If a fatal error occurs, it performs more initialization of DMA and interrupt controller circuits, tries to display an error message, complements the lower 6 bits of the POST code, sends the result to port 378, and halts the CPU, so numbers will flicker on the POST display with bit 6 on and the lower bits running from 0 upward. The codes start at 40 because a black box was used to monitor POST status at the parallel port. Bit 6 was set true (1) to alert the box the POST was starting.

Code	Meaning
40	CPU flags and register test failed (fatal)
41	BIOS ROM checksum test failed (fatal)
42	Disable pdma controller comd and test 8253 timer channel 1, mode 2, refresh counter (fatal); display sub-error code of 1 if interval is below window, 2 if above, and 3 if timer does not reply.
43	8237 DMA controller test failed (fatal)-master clear the controller, set the mask register, read the control registers, test all 8 read/writeable channel registers. Test registers 0-3 DMA address and count with FFFF then 0000.Set up channel 0 for 64K RAM address refresh. Set up memory-to-I/O transfer, unmask the RAM refresh, and let refresh begin for the first time. Set up the 8253 for proper refresh count. Test for unexpected DMA request (suberror 3), and init DMA channel 1 (not used), 2 (floppy), 3 (display), and init nibble latches. Check for proper DMA transfer into lowest 64K bank of RAM (suberror 4 if parity error).
44	8259 PIC test failed (halt)-init stack to lower 64K RAM area just tested, init and disable 8259A, set up interrupt vectors in RAM, set up software then hardware diagnostic interrupt vectors, test software interrupts, then hardware interrupts. Disable interrupts via 8259 mask register, check for hot interrupts, convert hot mask to IRQ number, save any error code, install interrupt vectors, initialize video, and display error messages (H:#, where # is the hot IRQ#).
45	Install real interrupt vectors, determine system configuration from switches, and initialize video mono and colour. Set video mode 3, clear screen, and display passing error messages for CPU, ROM, DMA, or PIC. Size and clear RAM at every 64K bank past the lowest 64K, displaying the tested RAM as test progresses. Display errors in form cc:y000:zzz:wwww:rrrr, where cc is the config number, y the failing segment, z the offset, w the written data and r the read data. Test MM58174 clock calendar, and display message if fails Test 8253 real time clock count capability, and tone generator. Display errors, halt if failure.
48	Send beep to display and initialize all basic hardware. Init 8041 keyboard controller, determine parallel port configurations and test their registers, determine serial 8250 and Z8530 configurations, check for game card, set up interrupt controller, set all 4 Z8530 serial controllers to 9600 baud, no parity, 1 stop and 8 data. Set up interrupt vectors, initialize RAM variables, clear the screen, initialize the hard disk controller, test for and initialize option ROMs, verify ROM checksums okay, initialize floppy disk controller, allow user to select alternate Z8000 processor if installed and perform INT 19 cold boot.

EISA 2.01

Port 278, 378, Or 3BC (i.e. printer ports)

Code	Meaning	Code	Meaning
01	Test CPU flags, registers. Initialize PIC	1E	Test IDTR and GDTR
02	Test memory refresh	1F	Test CMOS shutdown byte
03	Test CMOS RTC periodic interrupt	20	Test real/protected mode
04	Test gate A20 line	21	Check system memory configuration
05	Test mapping memory SRAM	22	Size memory

Code	Meaning	Code	Meaning
06	Test first 128K RAM. Stack has now been established	23	Test 640K base memory
07	Test for console presence and initialize	24	Verify base memory configuration
08	Verify system BIOS ROM checksum	25	Test extended memory (above 1 Mb)
09	Test 8042 keyboard controller Normal burn-in/manufacturing mode established	26	Verify extended memory configuration
0A	Test timer ratio	27	Check for contiguous extended memory
0B	Test CMOS RAM battery	28	Test cache memory. Extended BIOS data area created and POST errors logged
0C	Verify CMOS RAM checksum	29	Test protected mode instructions
0D	Test for unexpected NMI	2A	Test CMOS RAM
0E	Test interrupt controller #1	2B	Test real time clock
0F	Test interrupt controller #2	2C	Check calendar values
10	Test timer 1 counter 0	2D	Test keyboard/AUX device fuse
11	Test system control port B	2E	Test keyboard
12	Test system control port A	2F	Initialize keyboard typematic rate and delay
13	Verify checksum of NVRAM configuration	30	Test auxiliary device
14	Initialize system board	31	Test 80x87 math coprocessor
15	Initialize adapter	32	Test and initialize Weitek math coprocessor
16	Initialize ESC SCSI adapter	33	Run 1860 CPU basic and advanced diagnostics
17	Initialize system video	34	Test and configure serial ports
18	Test and copy shadow RAM. Video init-display banner and non-fatal errors	35	Test and configure parallel ports
19	Test DMA page registers	36	Detect game port
1A	Test DMA address registers	37	Test and initialize hard drives
1B	Test DMA count registers	38	Test and initialize floppy drives
1C	Test DMA mask registers	39	Scan for and pass control to adapter ROMs
1D	Test DMA stop registers. Initialize DMA controllers	3A	INT 19 boot-load operating system

PS/2 Compatible

Code	Meaning	Code	Meaning
01	Processor test	24	Watchdog timer test
02	Shutdown	25	Test RAM from 64K to 640K
03	Interrupt controller initialisation	26	Configure memory 640K
04	Refresh test	27	Text expansion memory
05	CMOS periodic interrupt test	28	Init ext BIOS data segment, log errors
06	Timer ratio	29	Configure memory above 1 Mb
07	Test first 64k RAM	2A	Dummy checkpoint
08	Test the KBC (8742)	2B	Test RAM parity
09	NMI test	2C	Test DMA page registers
0A	8254 test	2D	Test DMA controller base/current address registers
0B	Port 94h test	2E	Test DMA transfer count register
0C	Port 103h test	2F	Initialize DMA controller
0D	Port 102h test	30	Test PIO 61
0E	Port 96h test	31	Test keyboard
0F	Port 107h test	32	Initialize keyboard typematic rate and delay

Code	Meaning	Code	Meaning
10	Blank the screen	33	Test AUX device
11	KB/Aux device fuse check	34	Test advanced protected mode
12	CMOS battery test	35	Configure parallel ports
13	CMOS RAM checksum test	36	Configure 8250 serial ports
14	Extended CMOS checksum 0-8K	37	Configure coprocessor
15	System board and adapter initialisation	38	Configure game card
16	RAM test and initialisation	39	Configure and initialize hard disk
17	Protected mode register test	3A	Floppy disk configuration
18	CMOS RAM shutdown byte test	3B	Initialize ROM drivers
19	80286 protected mode test	3C	Display total memory and hard drives
1A	Video option ROM scan	3D	Final initialization, Checkpoints complete
1B	EPROM checksum test	3E	Detect and initialize parallel ports
1C	Interrupt controller #1 test	3F	Initialize hard drive and controller
1D	Interrupt controller #2 test	40	Detect and initialize math coprocessor
1E	Interrupt vector initialisation	41	Reserved
1F	CMOS RAM test	42	Initiate adapter ROM scan
20	Extended CMOS r/w test	CC	Unexpected processor exception occurred
21	CMOS clock test	DD	Save DDNIL status
22	Clock calendar test	EE	NMI handler shutdown
23	Dummy checkpoint	FF	INT 19 boot

PACKARD BELL

See Phoenix.

PHILIPS/MAGNAVOX/HEADSTART

Philips, Magnavox, and HeadStart use motherboards designed by Philips Home Electronics in Montreal. Most use a Philips-designed BIOS, although at least one of their portables uses one from Award Software. The beep pattern consists of a series of long and short beeps that correspond to the binary representation of the POST code where leading zeroes are omitted; a zero means a short and a one means a long beep. The various Philips platforms do not all execute the same POST tests.

Philips Platform Cross Reference

Platform	CPU	System Model/Name
Avenger	80286	Magnavox MaxStation 286, Magnum GL; Headstart Series 300
P3212	80286	Magnavox MaxStation 480, Headstart System 380
P 3239	8028680386SX	Magnavox Headstart/Maxstation/Magnum/Professional 1200, 48CD, 1600, 64CD, P160, SR16CD
P 3349	80386SX-20	Magnavox Headstart/Maxstation/Magnum/Professional SX20, 80CD
P3345	80386SX	Magnavox Maxstation 386SX, Magnum SX; Headstart Series 500
P33711	80386DX	Headstart/Maxstation/Magnum/Professional 3300

Code	Beeps0=sh 1=lng	Meanings (Port 80)
0A	1010	DMA page register write/read bad
10	1 0000	CMOS RAM read/write error (only after hard reset)
11	1 0001	System ROM BIOS checksum error
12	1 0010	Timer A error
13	1 0011	DMA controller A error
14	1 0100	DMA controller B error
15	1 0101	Memory refresh error
16	1 0110	Keyboard controller error
17	1 0111	Keyboard controller error
19	1 1001	Keyboard controller error
1C	1 1100	Base 64K RAM error
1D	1 1101	Base 64K RAM parity error
1F	1 1111	Orvonton LSI sync missing
21	10 0001	PVAM register error
25	10 0101	System options error
2B	10 1011	Video sync error (incorrect switch or CMOS RAM)
2C	10 1100	Video BIOS ROM error
2D	10 1101	Monochrome/colour configuration error
2E	10 1110	No video memory
35	11 0101	Interrupt controller error
36	11 0110	Byte swapper error
37	11 0111	NMI error
38	11 1000	Timer interrupt
39	11 1001	LSI timer halted
3A	11 1010	Main memory test error
3B	11 1011	Keyboard error
3C	11 1100	Keyboard interrupt error (only after hard reset)
3D	11 1101	DDNIL scan halted, cache disabled
40	100 0000	Diskette error
48	100 1000	Adapter card error
4c	100 1100	CMOS battery/checksum error (run SETUP)
4D	100 1101	System options error (run Setup)
52	101 0010	Keyboard controller error
6A	110 1010	Failure shadowing BIOS ROM
70	111 0000	Memory size configuration error (run SETUP)

PHOENIX

On 4.3 and above, the system will generate a code with four groups of beeps, with 1-4 per group. Micro channel ones send codes to 680.

Architecture	Typical Computer	POST Port
ISA	XT	60
	AT	80
	PS/2 25/30	90
EISA	Intel chipset	80
MCA	PS/2 50 up	68O

POST Procedures

Procedure	Meaning
CPU	Check internal operations e.g. ALE/IRQ status; Request; ALU and Memory Read/Write.
CMOS RAM	Test with walking-bit pattern.
ROM BIOS	Perform checksum on ROM BIOS where all bits are added and compared to a factory-set total.
PIT	Check to ensure interrupt requests are properly executed.
DMA	Check DMA from CPU to memory without BIOS. Also check page registers.
Base 64K	Check first 64K block.
Serial and Parallel	I/O data areas for any devices found are assigned; they are not tested.
PIC	Check that proper interrupt request levels are addressed.
Keyboard Controller	Check 8240 for proper operationluding scan code response and Gate A20 which allows CPU operation in protected mode.
CMOS	Check data within CMOS and compare to BIOS information. Failure of the extended area is often due to wrong data setup. Constant failure after resetting CMOS is either battery CMOS chip or RTC.
Video Controller	Test and initialise controller and ROM on the video adapter.
RTC	Check to ensure proper frequencies are on proper lines for the Video Colour CPU and DMA Frequency. Check RTC/PIT or system crystal.
CPU	Return From Protected Mode. CPU is put into protected mode and returns to the POST at the point indicated by the CMOS ROM data area byte 0F. Failure here is normally due to the CPU/keyboard controller/CMOS chip or an address line.
PIC	Test Counter 2.
NMI	Check the Non-Maskable Interrupt request vector for active status. Failure is normally due to the CMOS but could also be the BIOS IRQ or CPU chips.
Keyboard	Check for NumLock/Caps and Shift Keys.
Mouse	Initialise through the keyboard controller; this is only done if a mouse is present and it is initialised in this way.
RAM above 64K	Test in 64K blocks with a walking-bit pattern and parity enabled.
Fixed/Floppy Controllers	Test for proper response to BIOS calls.
Shadow RAM Areas	Look in CMOS for settings on which adapter or system ROMs are to be shadowed.
Option ROM	Look for ROM signatures of 55AA in extended memory then initialise the ROM and halt testing while internal checks are carried out.
External Cache	Check controller chip for external cache.
CPU Int Cache	
Hardware Adapters	Initialise and test video/floppy/hard I/O adapters/serial and parallel.
Cassette	Test internal or external cassette drives.
Boot Code Errors	Errors occurring after this point are normally a corrupt boot record.

2.52 BNP XT

Code	Meaning
01	Test 8253 timer
02	First 64K RAM failed
03	First 1K parity check failed
04	Initialize 8259 interrupt controller
05	Second 1K RAM test (BIOS data area) failed

BIOS Plus or v1.0 POST/Beep Codes

Only for BIOS PLUS or A286/A386/A486 Version 1.xx on an AT-class (80286 or higher) systems. Codes in the 50h range or beyond are chipset or platform specific, and will vary from system to system.

Code	Beeps	Meaning
01	none	CPU register test in progress.
02	1-1-3	CMOS write/read failure.
03	1-1-4	ROM BIOS Checksum Failure.
04	1-2-1	Programmable interval timer failure.
05	1-2-2	DMA Initialisation failure.
06	1-2-3	DMA page register write/read failure.
08	1-3-1	RAM refresh verification failure.
09	none	1st 64K RAM test in progress.
0A	1-3-3	1st 64K RAM chip or data line failure multi-bit.
0B	1-3-4	1st RAM odd/even logic failure.
0C	1-4-1	Address line failure 1st 64K RAM.
0D	1-4-2	Parity failure 1st 64K RAM.
10	2-1-1	Bit 0 1st 64K RAM failure.
11	2-1-2	Bit 1 1st 64K RAM failure.
12	2-1-3	Bit 2 1st 64K RAM failure.
13	2-1-4	Bit 3 1st 64K RAM failure.
14	2-2-1	Bit 4 1st 64K RAM failure.
15	2-2-2	Bit 5 1st 64K RAM failure.
16	2-2-3	Bit 6 1st 64K RAM failure.
17	2-2-4	Bit 7 1st 64K RAM failure.
18	2-3-1	Bit 8 1st 64K RAM failure.
19	2-3-2	Bit 9 1st 64K RAM failure.
1A	2-3-3	Bit A(10) 1st 64K RAM failure.
1B	2-3-2	Bit B(11) 1st 64K RAM failure.
1C	2-4-2	Bit C(12) 1st 64K RAM failure.
1D	2-4-2	Bit D(13) 1st 64K RAM failure.
1E	2-4-3	Bit E(14) 1st 64K RAM failure.
1F	2-4-4	Bit F(15) 1st 64K RAM failure.
20	3-1-1	Slave DMA register failure.
21	3-1-2	Master DMA register failure.
22	3-1-3	Master interrupt mask register failure.
23	3-1-4	Slave interrupt mask register failure.
25	none	Interrupt vector loading in progress.
27	3-2-4	8042 keyboard controller test failure.
28	none	CMOS power failure/checksum calculation in progress.
29	none	CMOS configuration validation in progress.
2B	3-3-4	Screen memory test failure.
2C	3-4-1	Screen initialisation failure.
2D	3-4-2	Screen retrace test failure.
2E	none	Search for video ROM in progress.
30	none	Screen believed running with video ROM.
31	none	Mono monitor believed operable.
32	none	Colour monitor (40 col) believed operable.
33	none	Colour monitor (80 col) believed operable.
34	4-2-1	Timer tick interrupt test in progress or failed (non-fatal).

Code	Beeps	Meaning
35	4-2-2	Shutdown failure (non-fatal).
36	4-2-3	Gate A20 failure (non-fatal).
37	4-2-4	Unexpected interrupt in protected mode (non-fatal).
38	4-3-1	Mem high address line fail at 01000-0A000 (non-fatal).
39	4-3-2	Mem high addr line fail at 100000-FFFFFF (non-fatal).
3A	4-3-3	Timer chip counter 2 failed (non-fatal).
3B	4-3-4	Time-of-day clock stopped
3C	4-4-1	Serial port test
3D	4-4-2	Parallel port test
3E	4-4-3	Maths coprocessor test
41	low 1-1-2	System board select bad
42	low 1-1-3	Extended CMOS RAM bad

PCI

Code	Meaning
02	If the CPU is in protected mode turn on A20 and pulse the reset line; forcing a shutdown 0.
04	On a cold boot save the CPU type information value in the CMOS.
06	Reset DMA controllers. Disable videos. Clear pending interrupts from RTC. Setup port B register.
08	Initialise chipset control registers to power on defaults.
0A	Set a bit in the CMOS that indicates POST; used to determine if the current configuration causes the BIOS to hang. If so default values will be used on next POST.
0C	Initialise I/O module control registers.
0E	External CPU caches are initialised. Cache registers are set to default.
10/12/14	Verify response of 8742.
16	Verify BIOS ROM checksums to zero.
18	Initialise all three of 8254 timers.
1A	Initialise DMA command register. Initialise 8 DMA channels.
1C	Initialise 8259 interrupt controller to :ICW4 needed; Cascade and edge-triggered mode.
20	Test DRAM refresh by polling refresh bit in PORTB.
22	Test 8742 keyboard controller. Send self test command to 8742 and await results. Also read the switch inputs from the 8742 and write the keyboard controller command byte.
24	Set ES segment register to 4 Gb
26	Enable Address Line A20
28	Autosize DRAM
2A	Clear first 64K of RAM
2C	Test RAM address lines
2E	Test first 64K bank of memory consisting of a chip address line test and a RAM test.
30/32	Find true MHz value
34	Clear CMOS diagnostic byte (register E). Check RTC and verify battery has not lost power. Checksum the CMOS and verify it has not been corrupted.
36/38/3A	External cache is autosized and its configuration saved for enabling later in POST.
3C	Configure advanced cache features. Configure external cache's configurable parameters.
3E	Read hardware configuration from keyboard controller
40	Set system power-on speed to rate determined by CMOS. If CMOS is invalid use a conservative speed.
42	Initialise interrupt vectors 0-77h to the BIOS general interrupt handler.
44	Initialise interrupt vectors 0-20h to proper values from the BIOS interrupt table.
46	Check copyright message checksum.
48	Check video configuration.

Code	Meaning
4A	Initialise both monochrome and colour graphics video adapters.
4C/4E	Display Copyright message.
50	Display CPU type and speed
52	Test for the self-test code if a cold start. When powered the keyboard performs a self-test and sends an AA if successful.
54	Initialise keystroke clicker during POST.
56	Enable keyboard
58	Test for unexpected interrupts. First do an STI for hot interrupts; secondly test NMI for unexpected interrupt. Thirdly enable parity checkers and read from memory checking for unexpected interrupt.
5A	Display prompt Press F2 to Enter Setup
5C	Determine and test the amount of memory available. Save the total memory size in the BIOS variable called bdaMemorySize.
5E	Perform address test on base memory. Following address lines are tested based on the memory size.
60	Determine and test the amount of extended memory available. Save the total extended memory size in the CMOS at CMOSExtended.
62	Perform an address line test on A0 to the amount of memory available. This test is dependent on the processor since the test will vary depending on the width of memory (16 or 32 bits). This test will also use A20 as the skew address to prevent corruption of the system memory.
68	External and CPU caches if present are enabled. Non-cacheable regions are configured if necessary.
6A	Display cache size on screen if non-zero.
6C	Display BIOS shadow status.
6E	Display the starting offset of the non-disposable section of the BIOS.
70	Check flags in CMOS and in the BIOS data area to see if any errors have been detected during POST. If so, display error messages on the screen.
72	Check status bits for configuration errors. If so display error messages on the screen.
74	Test RTC if the battery has not lost power. If the RTC is not running or the battery has lost powerset the incorrect time bit in register E of the CMOS.
76	Check status bits for keyboard errors. If so display error messages on the screen.
78	Check for stuck keys on the keyboard. If so display error messages on the screen.
7A	Enable keylock
7C	Set up hardware interrupt vectors
7E	Test coprocessor if present
80-82	Detect and install RS232 ports
84	Detect and install parallel ports
86-88	Initialise timeouts/key buffer/soft reset flag.
8A	Initialise extended BIOS data area and initialise the mouse.
8C	Initialise both floppy disks and display an error message if failure was detected. Both drives are checked so the appropriate diskette types are established in the BIOS data area.
8E	Hard disk autotype configuration
90	If the CMOS RAM is valid and intact and fixed disks are defined call the fixed disk init routine to initialise the fixed disk system and take over the appropriate interrupt vectors.
92-94	Disable A20 address line
96-98-	Scan for ROM BIOS extensions.
9E	Enable hardware interrupts
A0	Set time of day
A2	Set up NumLock indicator. Display a message if key switch is locked.
A4	Initialise typematic rate.
A6	Initialise hard disk autoparking.
A8	Erase F2 prompt.
AA	Scan for F2 key strokes.
AC	Check to see if SETUP should be executed.

Code	Meaning
AE	Clear ConfigFailedBit and InPostBit in CMOS.
B0	Check for POST errors
B2	Set/clear status bits to reflect POST complete.
B4	One beep.
B6	Check for password before boot.
B8	Clear global descriptor table (GDT).
BA	Initialise the screen saver.
BC	Clear parity error latch.
BE	Clear screen.
C0	Try to boot with INT 19
D0-D2	If an interrupt occurs before interrupt vectors have been initialised this interrupt handler will try to see if the interrupt caused was an 8259 interrupt and which one. If unknown, InterruptFlag will be FF. Otherwise it will contain the IRQ number that occurred
D4	Clear pending timer, kbd interrupts, transfer control to double word address at RomCheck.
D6-D8-DA	Return from extended block move.

Phoenix v3.07

see Quadtel.

ISA/EISA/MCA BIOS POST/Beep Codes (fatal)

Msg	Beeps	Meaning
01	none	CPU register test in progress.
02	1-1-3	CMOS write/read failure.
03	1-1-4	ROM BIOS Checksum Failure.
04	1-2-1	Programmable interval timer failure.
05	1-2-2	DMA Initialisation failure.
06	1-2-3	DMA page register write/read failure.
08	1-3-1	RAM refresh verification failure.
09	none	1st 64K RAM test in progress.
0A	1-3-3	1st 64K RAM chip or data line failure multi-bit.
0B	1-3-4	1st RAM odd/even logic failure.
0C	1-4-1	Address line failure 1st 64K RAM.
0D	1-4-2	Parity failure 1st 64K RAM.
0E	1-4-3	Fail-safe timer failure.
0F	1-4-4	Software NMI port failure.
10	2-1-1	Bit 0 1st 64K RAM failure.
11	2-1-2	Bit 1 1st 64K RAM failure.
12	2-1-3	Bit 2 1st 64K RAM failure.
13	2-1-4	Bit 3 1st 64K RAM failure.
14	2-2-1	Bit 4 1st 64K RAM failure.
15	2-2-2	Bit 5 1st 64K RAM failure.
16	2-2-3	Bit 6 1st 64K RAM failure.
17	2-2-4	Bit 7 1st 64K RAM failure.
18	2-3-1	Bit 8 1st 64K RAM failure.
19	2-3-2	Bit 9 1st 64K RAM failure.
1A	2-3-3	Bit A 1st 64K RAM failure.
1B	2-3-2	Bit B 1st 64K RAM failure.

Msg	Beeps	Meaning
1C	2-4-2	Bit C 1st 64K RAM failure.
1D	2-4-2	Bit D 1st 64K RAM failure.
1E	2-4-3	Bit E 1st 64K RAM failure.
1F	2-4-4	Bit F 1st 64K RAM failure.
20	3-1-1	Slave DMA register failure.
21	3-1-2	Master DMA register failure.
22	3-1-3	Master interrupt mask register failure.
23	3-1-4	Slave interrupt mask register failure.
25	none	Interrupt vector loading in progress.
27	3-2-4	Keyboard controller test failure.
28	none	CMOS pwr failure; checksum calculation in progress.
29	none	CMOS RAM configuration validation in progress.
2B	3-3-4	Screen memory test failure.
2C	3-4-1	Screen initialisation failure.
2D	3-4-2	Screen retrace test failure.
2E	none	Search for video ROM in progress.
30	none	Screen believed running with video ROM.
31	none	Mono monitor believed operable.
32	none	Colour monitor (40 col) believed operable.
33	none	Colour monitor (80 col) believed operable.

ISA/EISA/MCA BIOS POST/Beep Codes (non-fatal)

Non-fatal if manufacturing jumper is on.

Msg	Beeps	Meaning
34	4-2-1	No time tick.
35	4-2-2	Shutdown test in progress or failure.
36	4-2-3	Gate A20 failure.
37	4-2-4	Unexpected interrupt in protected mode.
38	4-3-1	Memory high address line fail at 01000-0A000. Also RAM test in progress or address failure >FFFH.
39	4-3-2	Memory high address line failure at 100000-FFFFFF.
3A	4-3-3	Interval Timer channel 2 test or failure.
3B	4-3-4	Time-of-day clock test or failure.
3C	4-4-1	Serial port test or failure.
3D	4-4-2	Parallel port test or failure.
3E	4-4-3	Maths coprocessor test
3F		Cache test (Dell)
41	lw 1-1-2	System board select bad (Micro Channel only)
42	Low 1-1-3	Extended CMOS RAM bad (Micro Channel only)

PicoBIOS v4.0 R6/UMC Chipset PCI

Beeps	Code	Meaning
1-1-1-3	02	Verify Real Mode
1-1-2-1	04	Get CPU type
1-1-2-3	06	Initialize system hardware
1-1-3-1	08	Initialize chipset registers with initial POST values

Beeps	Code	Meaning
1-1-3-2	09	Set in POST flag
1-1-3-3	0A	Initialize CPU registers
1-1-4-1	0C	Initialize cache to initial POST values
1-1-4-3	0E	Initialize I/O
1-2-1-1	10	Initialize Power Management
1-2-1-2	11	Load alternate registers with initial POST values
1-2-1-3	12	Jump to UserPatch0
1-2-2-1	14	Initialize keyboard controller
1-2-2-3	16	BIOS ROM checksum
1-2-3-1	18	8254 timer initialization
1-2-3-3	1A	8237 DMA controller initialization
1-2-4-1	1C	Reset Programmable Interrupt Controller
1-3-1-1	20	Test DRAM refresh
1-3-1-3	22	Test 8742 Keyboard Controller
1-3-2-1	24	Set ES segment to register to 4 GB
1-3-3-1	28	Autosize DRAM
1-3-3-3	2A	Clear 512K base RAM
1-3-4-1	2C	Test 512 base address lines
1-3-4-3	2E	Test 512K base memory
1-4-1-3	32	Test CPU bus-clock frequency
1-4-2-1	34	CMOS RAM read/write failure (check ISA card seating)
1-4-2-4	37	Reinitialize the chipset
1-4-3-1	38	Shadow system BIOS ROM
1-4-3-2	39	Reinitialize the cache
1-4-3-3	3A	Autosize cache
1-4-4-1	3C	Configure advanced chipset registers
1-4-4-2	3D	Load alternate registers with CMOS values
2-1-1-1	40	Set Initial CPU speed
2-1-1-3	42	Initialize interrupt vectors
2-1-2-1	44	Initialize BIOS interrupts
2-1-2-3	46	Check ROM copyright notice
2-1-2-4	47	Initialize manager for PCI Options ROMs
2-1-3-1	48	Check video configuration against CMOS
2-1-3-2	49	Initialize PCI bus and devices
2-1-3-3	4A	Initialize all video adapters in system
2-1-4-1	4C	Shadow video BIOS ROM
2-1-4-3	4E	Display copyright notice
2-2-1-1	50	Display CPU type and speed
2-2-1-3	52	Test keyboard
2-2-2-1	54	Set key click if enabled
2-2-2-3	56	Enable keyboard
2-2-3-1	58	Test for unexpected interrupts
2-2-3-3	5A	Display prompt Press F2 to enter SETUP
2-2-4-1	5C	Test RAM between 512 and 640k
2-3-1-1	60	Test expanded memory
2-3-1-3	62	Test extended memory address lines
2-3-2-1	64	Jump to UserPatch1
2-3-2-3	66	Configure advanced cache registers
2-3-3-1	68	Enable external and CPU caches

Beeps	Code	Meaning
2-3-3-2	69	Initialise SMI handler
2-3-3-3	6A	Display external cache size
2-3-4-1	6C	Display shadow message
2-3-4-3	6E	Display non-disposable segments
2-4-1-1	70	Display error messages
2-4-1-3	72	Check for configuration errors
2-4-2-1	74	Test real-time clock
2-4-2-3	76	Check for keyboard errors
2-4-4-1	7C	Set up hardware interrupts vectors
2-4-4-3	7E	Test coprocessor if present
3-1-1-1	80	Disable onboard I/O ports
3-1-1-3	82	Detect and install external RS232 ports
3-1-2-1	84	Detect and install external parallel ports
3-1-2-3	86	Re-initialize onboard I/O ports
3-1-3-1	88	Initialize BIOS Data Area
3-1-3-3	8A	Initialize Extended BIOS Data Area
3-1-4-1	8C	Initialize floppy controller
3-2-1-1	90	Initialize hard-disk controller
3-2-1-2	91	Initialize local-bus hard-disk controller
3-2-1-3	92	Jump to UserPatch2
3-2-2-1	94	Disable A20 address line
3-2-2-3	96	Clear huge ES segment
3-2-3-1	98	Search for option ROMs
3-2-3-3	9A	Shadow option ROMs
3-2-4-1	9C	Set up Power Management
3-2-4-3	9E	Enable hardware interrupts
3-3-1-1	A0	Set time of day
3-3-1-3	A2	Check key lock
3-3-3-1	A8	Erase F2 prompt
3-3-3-3	AA	Scan for F2 key stroke
3-3-4-1	AC	Enter SETUP
3-3-4-3	AE	Clear in-POST flag
3-4-1-1	B0	Check for errors
3-4-1-3	B2	POST done--prepare to boot operating system
3-4-2-1	B4	One beep
3-4-2-3	B6	Check password (optional)
3-4-3-1	B8	Clear global descriptor table
3-4-4-1	BC	Clear parity checkers
3-4-4-3	BE	Clear screen (optional)
3-4-4-4	BF	Check virus and backup reminders
4-1-1-1	C0	Try to boot with INT 19
4-2-1-1	D0	Interrupt handler error
4-2-1-3	D2	Unknown interrupt error
4-2-2-1	D4	Pending interrupt error
4-2-2-3	D6	Initialize option ROM error
4-2-3-1	D8	Shutdown error
4-2-3-3	DA	Extended Block Move
4-2-4-1	DC	Shutdown 10 error

FLASH BIOS INTEGRITY TEST

4-3-1-3	E2	Initialize the chipset
4-3-1-4	E3	Initialize refresh counter
4-3-2-1	E4	Check for Forced Flash
4-3-2-2	E5	Check HW status of ROM
4-3-2-3	E6	BIOS ROM is OK
4-3-2-4	E7	Do a complete RAM test

FLASH RECOVERY

4-3-3-1	E8	Do OEM initialization
4-3-3-2	E9	Initialize interrupt controller
4-3-3-3	EA	Read in bootstrap code
4-3-3-4	EB	Initialize all vectors
4-3-4-1	EC	Boot the Flash program
4-3-4-2	ED	Initialize the boot device
4-3-4-3	EE	Boot code was read OK

v4.0 R6

Code	Meaning	Code	Meaning
02	Verify Real Mode	6B	Load custom defaults (optional)
03	Disable NMI	6C	Display shadow area message
04	Get CPU type	6E	Show possible high address UMB recovery
06	Init system hardware	70	Display error messages
08	Init chipset registers with initial POST values	72	Check for configuration errors
09	Set IN POST flag	76	Check for keyboard errors
0A	Init COU registers	7C	Set up hardware interrupt vectors
0B	Enable CPU cache	7E	Init copro if present
0C	Init caches to initial POST values	80	Disable onboard super I/O ports and IRQs
0E	Init I/O component	81	Late POST device inti
0F	Init local bus IDE	82	Detect and install external RS232 ports
10	Init power management	83	Configure non-MCD IDE controllers
11	Load alternate registers with initial POST values	84	Detect and install external parallel ports
12	Restore CPU control word during warm boot	85	Init PC-compatible PnP ISA devices
13	Init PCI bus mastering devices	86	Re-initialise onboard I/O ports
14	Init keyboard controller	87	Set motherboard configurable devices
16	BIOS ROM checksum (beep 1-2-2-3)	88	Init BIOS data area
17	Init cache before memory autosize	89	Enable NMIs
18	8254 timer init	8A	Init BIOS extended data area
1A	8237 DAM controller init	8B	Test/init PS/2 mouse
1C	Reset programmable interrupt controller	8C	Init floppy controller
20	Test DRAM refresh (beep 1-3-1-1)	8F	Determine number of ATA drives (optional)
22	Test 8742 controller (beep 1-3-1-3)	90	Init HD controller
24	Set ES segment register to 4 Gb	91	Init local bus HD controller
26	Enable A20 line	92	Jump to Userpatch2
28	Autosize DRAM	93	Build MPTABLE for multi-processor boards

Code	Meaning	Code	Meaning
29	Init POST memory manager	95	Install CD ROM for boot
2A	Clear 512K base RAM	96	Clear huge ES segment register
2C	RAM failure on line XXXX (beep 1-3-4-1)	97	Fix up multiprocessor table
2E	RAM failure on data bits xxxx of low byte of memory bus (beep 1-3-4-3)	98	Search for option ROMs (beep 1-2)
2F	Enable cache before system BIOS shadow	99	Check for SMART Drive (optional)
30	RAM failure on data bits xxxx of high byte of memory bus (beep 1-4-1-1)	9A	Shadow Option ROMs
32	Test CPU bus clock frequency	9C	Set up power management
33	Init Phoenix Dispatch Manager	9D	Init security engine (optional)
36	Warm start shut down	9E	Enable hardware interrupts
38	Shadow system BIOS ROM	9F	Determine number of ATA and SCSI drives
3A	Autosize cache	A0	Set time of day
3C	Advanced conguration of chipset registers	A2	Check key lock
3D	Load alternate registers with CMOS values	A4	Init typematic rate
42	Init interrupt vectors	A8	Erase F2 prompt
45	POST device init	AA	Scan for F2 keystroke
46	Check ROM copyright notice (beep 2-1-2-3)	AC	Enter setup
48	Check video configuration against CMOS	AE	Clear boot flag
49	Init PCI bus and devices	B0	Check for errors
4A	Init all video adapters	B2	POST done, prepare to boot OS
4B	QuietBoot start (optional)	B4	One short beep before boot
4C	Shadow Video BIOS ROM	B5	Terminate Quickboot (optional)
4E	Display BIOS copyright notice	B6	Check password (optional)
50	Display CPU type and speed	B9	Prepare Boot
51	Init EISA board	BA	Init DMI parameters
52	Test keyboard	BB	Init PnP Option ROMs
54	Set key click if enabled	BC	Clear parity checkers
58	Test for unexpected interrupts (2-2-3-1)	BD	Display multiboot menu
59	Init POST display service	BE	Clear Screen (optional)
5A	Display prompt "Press F2 to enter setup"	BF	Check virus and backup reminders
5B	Disable CPU cache	C0	Try to boot with INT 19
5C	Test RAM between 512K and 640K	C1	Init POSR error message (PEM)
60	Test expanded memory	C2	Init error logging
62	Test extended memory address lines	C3	Init error display function
64	Jump to user patch 1	C4	Init system error handler
66	Configure advanced cache registers	C5	PnPnd dual CMOS (optional)
67	Init multi processor APIC	C6	Init notebook docking (optional)
68	Enable external and CPU caches	C7	Init notebook docking late
69	Setup SMM area	C8	Force Check (optional)
6A	Display external L2 cache size	C9	Extended Checksum (optional)

FOR BOOT BLOCK IN FLASH ROM

Code	Meaning	Code	Meaning
E0	Init chipset	EA	Init OEM special code
E1	Init bridge	EB	Init PIC and DMA
E2	Init CPU	EC	Init memory type
E3	Init system timer	ED	Init memory size

Code	Meaning	Code	Meaning
E4	Init system I/O	F0	Init interrupt vectors
E5	Check force recovery boot	F1	Init RTC
E6	Checksum BIOS ROM	F2	Init video
E7	Go to BIOS	F3	Init system management mode
E8	Set huge segment	F4	Out put 1 beep before boot
E9	Init multi-processor	F5	Boot to mini DOS
EE	Shadow boot block	F6	Clear Huge Segment
EF	System memory test	F7	Boot to full DOS

V4 Rel 6

Code	Meaning	Code	Meaning
000h	TP_NULL	045h	TP_DEVICE_INIT
001h	TP_IPMI_INIT	046h	TP_COPYRIGHT
002h	TP_VERIFY_REAL	047h	TP_I2O_INIT
003h	TP_DISABLE_NMI	048h	TP_CONFIG
004h	TP_GET_CPU_TYPE	049h	TP_PCI_INIT
006h	TP_HW_INIT	04Ah	TP_VIDEO
007h	TP_CS_BIOS_DESHAD	04Bh	TP_QUIETBOOT_START
008h	TP_CS_INIT	04Ch	TP_VID_SHADOW
009h	TP_SET_IN_POST	04Eh	TP_CR_DISPLAY
00Ah	TP_CPU_INIT	04Fh	TP_MULTBOOT_INIT
00Bh	TP_CPU_CACHE_ON	050h	TP_CPU_DISPLAY
00Ch	TP_CACHE_INIT	051h	TP_EISA_INIT
00Eh	TP_IO_INIT	052h	TP_KB_TEST
00Fh	TP_FDISK_INIT	054h	TP_KEY_CLICK
010h	TP_PM_INIT	055h	TP_USB_INIT
011h	TP_REG_INIT	056h	TP_ENABLE_KB
012h	TP_RESTORE_CR0	057h	TP_1394_INIT
013H	TP_PCI_BM_RESET	058h	TP_HOT_INT
014h	TP_8742_INIT	059h	TP_PDS_INIT
016h	TP_CHECKSUM	05Ah	TP_DISPLAY_F2
017h	TP_PRE_SIZE_RAM	05Bh	TP_CPU_CACHE_OFF
018h	TP_TIMER_INIT	05Ch	TP_MEMORY_TEST
01Ah	TP_DMA_INIT	05Eh	TP_BASE_ADDR
01Ch	TP_RESET_PIC	060h	TP_EXT_MEMORY
020h	TP_REFRESH	062h	TP_EXT_ADDR
022h	TP_8742_TEST	064h	TP_USERPATCH1
024h	TP_SET_HUGE_ES	066h	TP_CACHE_ADVNCD
026h	TP_ENABLE_A20	067h	TP_MP_INIT_MIN
028h	TP_SIZE_RAM	068h	TP_CACHE_CONFIG
029h	TP_PMM_INIT	069h	TP_PM_SETUP_SMM
02Ah	TP_ZERO_BASE	06Ah	TP_DISP_CACHE
02Bh	TP_ENH_CMOS_INIT	06Bh	TP_CUST_DFLT
02Ch	TP_ADDR_TEST	06Ch	TP_DISP_SHADOWS
02Eh	TP_BASERAML	06Eh	TP_FAST_ZERO
02Fh	TP_PRE_SYS_SHADOW	070h	TP_ERROR_MSGS
030h	TP_BASERAMH	072h	TP_TEST_CONFIG

Code	Meaning	Code	Meaning
032h	TP_COMPUTE_SPEED	074h	TP_RTC_TEST
033h	TP_PDM_INIT	076h	TP_KEYBOARD
034h	TP_CMOS_TEST	07Ah	TP_KEYLOCK
035h	TP_REG_REINIT	07Ch	TP_HW_INTS
036h	TP_CHK_SHUTDOWN	07Dh	TP_ISM_INIT
037h	TP_CS_REINIT	07Eh	TP_COPROC
038h	TP_SYS_SHADOW	080h	TP_IO_BEFORE
039h	TP_CACHE_REINIT	0BDh	TP_BOOT_MENU
03Ah	TP_CACHE_AUTO	0BEh	TP_CLEAR_SCREEN
03Bh	TP_DBGSRV_INIT	0BFh	TP_CHK_RMDR
03Ch	TP_ADV_CS_CONFIG	0C0h	TP_INT19
03Dh	TP_ADV_REG_CONFIG	0C1h	TP_PEM_INIT
03Eh	TP_READ_HW	0C2h	TP_PEM_LOG
03Fh	TP_ROMPILOT_MEMORY	0C3h	TP_PEM_DISPLAY
040h	TP_SPEED	0C4h	TP_PEM_SYSER_INIT
041h	TP_ROMPILOT_INIT	0C5h	TP_DUAL_CMOS
042h	TP_VECTOR_INIT	0C6h	TP_DOCK_INIT
044h	TP_SET_BIOS_INT	0C7h	TP_DOCK_INIT_LATE
08Ch	TP_FLOPPY	0C8h	TP_FORCE
08Eh	TP_AUTOTYPE	0C9h	TP_EXT_CHECKSUM
08Fh	TP_FDISK_FAST_PREINIT	0CAh	TP_SERIAL_KEY
090h	TP_FDISK	081h	TP_LATE_DEVICE_INIT
091h	TP_FDISK_FAST_INIT	082h	TP_RS232
092h	TP_USERPATCH2	083h	TP_FDISK_CFG_IDE_CTRLR
093h	TP_MP_INIT	084h	TP_LPT
095h	TP_CD	085h	TP_PCI_PCC
096h	TP_CLEAR_HUGE_ES	086h	TP_IO_AFTER
097h	TP_MP_FIXUP	087h	TP_MCD_INIT
098h	TP_ROM_SCAN	088h	TP_BIOS_INIT
099h	TP_FDISK_CHECK_SMART	089h	TP_ENABLE_NMI
09Ah	TP_MISC_SHADOW	08Ah	TP_INIT_EXT_BDA
09Bh	TP_PMCPUSPEED	08Bh	TP_MOUSE
09Ch	TP_PM_SETUP	0CDh	TP_PCMATA
09Dh	TP_SECURITY_INIT	0CEh	TP_PEN_INIT
09Eh	TP_IRQS	0CFh	TP_XBDA_FAIL
09Fh	TP_FDISK_FAST_INIT2	0D1h	TP_BIOS_STACK_INIT
0A0h	TP_TIME_OF_DAY	0D3h	TP_SETUP_WAD
0A2h	TP_KEYLOCK_TEST	0D4h	TP_CPU_GET_STRING EQU
0A4h	TP_KEY_RATE	0D5h	TP_SWITCH_POST_TABLES
0A8h	TP_ERASE_F2	0C1h	TP_CHKBOOTTYPE
0AAh	TP_SCAN_FOR_F2	0C2h	TP_SAVEBOOTTYPE
0ACh	TP_SETUP_CHECK	0C3h	TP_CHKREQBOOTTYPE
0AEh	TP_CLEAR_BOOT	0C4h	TP_HOTKEY_START
0B0h	TP_ERROR_CHECK	0C5h	TP_HOTKEY_END
0B1h	TP_ROMPILOT_UNLOAD	0C6h	TP_CONSOLE_INIT
0B2h	TP_POST_DONE	0C7h	TP_CONSOLE_COMPORT
0B3h	TP_ENH_CMOS_STORE	0C8h	TP_A20_TEST
0B4h	TP_ONE_BEEP	0C9h	TP_EISA_BEFORE_INIT
0B5h	TP_QUIETBOOT_END	0CAh	TP_EISA_AFTER_INIT

Code	Meaning	Code	Meaning
0B6h	TP_PASSWORD	0CBh	TP_SAVE_MEMCFG
0B7h	TP_ACPI	0CCh	TP_RESTORE_MEMCFG EQU
0B8h	TP_SYSTEM_INIT	0CDh	TP_CONSOLE_VECTOR EQU
0B9h	TP_PREPARE_BOOT	0CEh	TP_ERRLOG_INIT
0Bah	TP_DMI	0CFh	TP_ERRLOG_MSG
0BBh	TP_INIT_BCVS	0CDh	TP_PCMATA
0BCh	TP_PARITY		

QUADTEL

v3.07 AT BIOS (Phoenix 3.07)

Code	Meaning	Code	Meaning
02	Flag test	4A	Start second protected mode test
04	Register test	4C	Verify LDT instruction
06	System hardware initialisation	4E	Verify TR instruction
08	Initialise chipset registers	50	Verify LSL instruction
0A	BIOS ROM checksum	52	Verify LAR instruction
0C	DMA page register test	54	Verify VERR instruction
0E	8254 timer test	56	Unexpected exception
10	8254 timer initialisation	58	Address line 20 test
12	8237 DMA controller test	5A	Keyboard ready test
14	8237 DMA initialisation	5C	Determine AT or XT keyboard
16	Initialise 8259/reset coprocessor	5E	Start third protected mode test
18	8259 interrupt controller test	60	Base memory test
1A	Memory refresh test	62	Base memory address test
1C	Base 64K address test	64	Shadow memory test
1E	Base 64K memory test	66	Extended memory test
20	Base 64K test (upper 16 bits) for 386s	68	Extended address test
22	8742 keyboard self test	6A	Determine memory size
24	MC 146818 CMOS test	6C	Display error messages
26	Start first protected mode test	6E	Copy BIOS to shadow memory
28	Memory sizing test	70	8254 clock test
2A	Autosize memory chips	72	MC 146818 RTC test
2C	Chip interleave enable test	74	Keyboard stuck key test
2E	First protected mode test exit	76	Initialise hardware interrupt vectors
30	Unexpected shutdown	78	Maths coprocessor test
31	DDNIL bit scan failure	7A	Determine COM ports available
32	System board memory size	7C	Determine LPT ports available
34	Relocate shadow RAM if configured	7E	Initialise BIOS data area
36	Configure EMS system	80	Determine floppy/fixed disk controller
38	Configure wait states	82	Floppy disk test
3A	Retest 64K base RAM	84	Fixed disk test
3C	CPU speed calculation	86	External ROM scan
3E	Get switches from 8042	88	System key lock test
40	Configure CPU speed	8A	Wait for <F1> key pressed

Code	Meaning	Code	Meaning
42	Initialise interrupt vectors	8C	Final system initialisation
44	Verify video configuration	8E	Interrupt 19 boot loader
46	Initialise video system	B0	Unexpected interrupt before or after boot.
48	Test unexpected interrupts		

16K XT

Code	Meaning
03	Test flag register
06	Test CPU Register
09	Initialise system hardware
0C	Test BIOS ROM checksum
0F	Initialise 8237 DMA page register
12	Test 8237 address and count registers
15	Initialise 8237 DMA
18	Test 8253 timer
1B	Initialise 8253 timer
1E	Start memory refresh test
21	Test base 64K RAM, Cycling POST display shows code, upper then lower bytes of failing address
24	Set up common INT temp stack
27	Initialize 8259 interrupt controller
2A	Test interrupt mask register
2D	Test for hot (unexpected) interrupt
30	Test V40 DMA if present
31	Test for DDNIL bits present
33	Verify system clock interrupt
36	Test keyboard
39	Set up interrupt table
3C	Read system configuration switches
3F	Test video
42	Determine COM ports available
45	Determine LPT ports available
48	Determine if game port available
4B	Display copyright message
4E	Calculate CPU speed
54	Test system memory
55	Test floppy drive
57	Initialize system before boot
5A	Call Interrupt 19 boot loader

SUPERSOFT

PC/XT/AT

	XT	AT
11	CPU register or logic error	CPU register or logic
12	ROM POST checksum error	ROMPOST A checksum error
13	8253 timer channel 0 error	ROMPOST B checksum error
14	8253 timer channel 1 error	8254 timer channel 0 error
15	8253 timer channel 2 error	8254 timer channel 1 error
16	8237A DMA controller error	8254 timer channel 2 error
17	8255 parity error detected	8237A DMA controller 1 err
18	16K critical RAM region error	8237A DMA controller 2 err
19	Memory refresh error	DMA page registers error
1A	-	8042 parity error detected
21	8259 Interrupt controller error	16K critical RAM region
22	Unexpected interrupt detected	Memory refresh error
23	Interrupt 0 (timer) error	CPU protected mode error
24	Nonmaskable interrupt error	8259 Interrupt controller 1 err
25	MDA video memory error	8259 Interrupt controller 2 err
26	CGA video memory error	Unexpected interrupt detected
27	EGA/VGA memory error	Interrupt 0 (timer) error
28	8087 math chip error	CMOS real time clock error
29	Keyboard controller error	Nonmaskable interrupt error
2A	-	8Ox87 math chip error
31	Keyboard scan lines/stuck key	Keyboard controller error
32	Floppy controller error	Stuck key or CMOS RAM err
33	Floppy disk read error	Floppy controller error
34	Memory error at address x	Floppy disk read error
35	Slow refresh, address x	MDA video memory error
36, 37	-	CGA, EGA/VGA RAM error
38	-	BIOS checksum error
41	BIOS checksum error	Memory error at address x
42	BASIC ROM 1 checksum	Slow refresh, address x
43-45	BASIC ROM 2, 3, 4	Display pass count
59	No monitor	No monitor

TANDON

Slimline 286, 386SX and 486; 486 EISA

Type A AT 29 Feb 1988

Code	Meaning
01	Test 80286 CPU flags and registers
02	Test BIOS ROM checksum
03	Test MC146818 CMOS RAM battery (RTC)
04	Test 8254 timer
05	8254 timer test failed
06	Initialize RAM refresh
07	Test first 16K RAM
08	Initialize cold boot interrupt vectors
09	Test 8259 interrupt controller and interrupt vectors
0A	Fill in temporary interrupt vectors
0B	Initialize interrupt vector table 1
0C	Initialize interrupt vector table 2
0D	Initialize fixed disk vector
0E	Interrupt vector test failed
0F	Clear keyboard controller input buffer
10	Keyboard controller input buffer clearing failed
11	Run keyboard controller self-test
12	Initialize equipment check data area
13	Determine presence of and install 80287 math coprocessor
14	Test MC146818 CMOS RAM disk value range
15	Test for and install parallel port
16	Test for and install serial port
17	Invoke INT 19 to boot operating system

Type B AT-1992

Code	Meaning
01	Cold boot started
06	Initialize chipset if any
07	Warm boot entry. About to start 8042 keyboard controller self-test
08	Part of cold boot keyboard initialization passed
09	Keyboard self-test finished. Test ROM BIOS checksum.
0A	Test CMOS RAM battery level
0B	Save CMOS RAM battery condition in CMOS diagnostic/status register
0C	Finished saving CMOS RAM battery condition
0D	Test 8254 PIT. Disable RAM parity, I/O parity, DMA controllers, and speaker; enable timer channel 2.
0E, AA, xx	8245 test failed. xx is the failing channel number.
0F	Initialize 8254 timer channels (0 to mode 3 for 55 ms square wave, 1 to mode 2 as rate generator for refresh) and conduct memory refresh test.
10	Refresh test failed
11	Test base 64K RAM and fill with zeros
12	64K RAM test failed. 3 long beeps and halt.

Code	Meaning
13	RAM test passed
14	Set up stack, disable mappers for systems that support EMS drivers (warm boot), initialize battery beep flag parameters for notebook, perform read/write test of CMOS , enable error message if failed.
15	CMOS RAM read/write test complete
16	Calculating CPU speed; may set to low if CMOS RAM failed
18	Test and initialize both 8259 interrupt controllers
1A	8259 initialization complete
1B	Install interrupt handler and vector for INT 0F to check for unexpected (spurious) interrupts. Halt if spurious interrupt occurs.
1C	Spurious interrupt did not occur (test pass). Test 8254 timer channel 0, IRQ0, and INT8 tests.
1D	Error. Timer 0 interrupt did not occur when expected. Halt system.
1E	Both 8259 interrupt controllers passed the tests
20	Set up interrupt vectors 02-1F
21	Set up interrupt vectors 70-77
22	Clear interrupt vectors for 41 and 46 (disk parameter pointers).
23	Read 8042 self-test result, DMA page reg ch 2 (port 81).
24	Test for proper 8042 self-test result (55).
25	Error: Keyboard controller self-test failed, display message and halt.
26	Keyboard controller self-test passed
27	Confirm DMA working; prepare DMA channel 2 for floppy data transfer
28	Reinitialize video (cold boot)
29	Reinitialize video with cursor off (warm boot)
2A	Video parameters are initialized
2B	Enable NMI and I/O channel check, disable 8254 timer channel 2 and speaker
2C	Run RAM test to determine size of RAM
2D	RAM sizing complete
2E	Send reset command to keyboard controller to initiate a keyboard scan cycle
2F	Keyboard has been initialized. Initialize the CMOS RTC
30	CMOS RTC has been initialized. Initialize on-board floppy if any
31	Install the hard disk controller
32	Disk controller has been installed; prepare DMA channel 2 for floppy transfers
33	Perform equipment check and initialize numeric data processor (math chip)
34	Install the serial/parallel ports
35	Test CMOS RAM battery level
36	Check for keypress-Esc=Setup, Spacebar=menu; do speed beeps 2=high, l=low
37	Enable 8254 timer channel 0 for system tick, enable keyboard and slave interrupt controller 8259 #2
38	Timer tick, keyboard and 8259 #2 enabled; enable/disable cache per CMOS RAM
39	Enable keyboard interface and interrupts. Go to Setup as necessary; shadow ROMs as appropriate.
3A	Setup finished, so clear the screen and display Please Wait message
3B	Test the fixed and floppy drives
3C	Scan for and invoke the adapter ROMs in C800-E000
3D	Turn off Gate A20; restore vectors 3bh-3fh with temporary interrupt service routines.
3E	Gate A20 is turned off
3F	Invoke INT19 to boot operating system.

These accompanied by 5 long beeps:

Code	Meaning
BF	486-based, 386SX/20c or 386SX/25c processor module boards are used in a system where the WD76C10 chipset is not revision F or above.
CF	CPU on a 486-based processor module has failed its internal self-test.
DF	386SX/20c or 386SX/25c module board failed correctly to initialize its on-board cache (bad cache RAM. illegal configuration, etc., or unknown module ID).
EF	Extended CMOS RAM within the WD76C10 chipset failed its self-test

486 EISA-10 Oct 1989

Code	Meaning
	Power on or system reset: enable 8042, RTC; disable 82C601 chip serial, parallel, floppy, hard drive, NMI; check 8042 status.
AA, 01, xx	Show 80486 BIST (built-in self-test) result: xx=00 if OK, FF if not.
01	Disable cache, enable ROM, high speed on, turn off caches, disable EISA NMIs, set master and slave IRQs to edge-triggered, disable reset chaining. disable 82C601 chip but set it valid.
05	Initialize address decoder, 640K RAM; set BIOS as cacheable, enable extended memory.
06	Clear Shutdown Flag.
07	8042 and keyboard test: wait till 8042 buffer empty, disable 8042 command, read 8042 output buffer, set response OK to DMA page reg channel 2.
08	Send 8042 NOP command, self-test command; get 8042 self-test result, send to DMA page reg channel 2.
AA, 01, xx	Show 8042 self-test result: xx=55 if OK
09	Test BIOS ROM checksum; 3 short beeps and halt if bad
0A	Read CMOS registers 3 times to clear pending RTC interrupts, and disable them. Check battery.
0B	Bad CMOS RAM battery.
0C	Send command to port 61 to disable parity and speaker, enable timer; disable DMA.
0D	Test 8254 counter timer: set all 3 counters to mode 3 (square wave), start them and read the counts.
0E	A counter timer is bad (at least one is 0 and not counting).
AA, 01, xx	Show failing counter address (xx = 40, 41, or 42), then beep L-S-L-S and halt.
0F	Enable and check memory refresh (set timer 1 to mode 2 for 15 microsecond refresh, and turn on DMA to perform it); delay 1 ms and check bit 4 of port 61 for 0-to-1 toggle.
10	Memory refresh failed (no toggle); beep short-long-short, and halt.
11	Check and clear the first 64K of RAM in real mode: disable NMI, clear parity latches, fill 64K with 5555 and check it, then AAAA and check it, then 0000.
AA, 06, mmnn, oopp, qqrr	First 64K memory test failed. mmnn=location lsb, msb; oopp= value read lsb, msb; qqrr=value expected lsb, msb.
AA, 01, xx	Test port 61 for parity error (bits 7, 6=1) and display xx=value read from port 61 if parity error occurred.
12	First 64K memory test failed. Clear parity latches, give 3 long beeps, and halt.
13	First 64K memory test passed.
14	Reset warm boot flag (40:72) and test CMOS. Turn off caches, shadow BIOS, set speed high, calculate high speed and initialize GP flag, set speed low and turn off cache if CMOS not good or speed not high, otherwise turn on cache and set speed high.
16	Check Shutdown Flag 123x.
17	Reset was cold boot. Set 40:e9 bit 7 (disk_status).
18	Prepare 8259 interrupt controllers; send FF to mask register and check.
19	Interrupt controller initialization failed; initialize video, display the error message, and halt.
1A	Test interrupt controller: set all 256 ints to slipped interrupt vector. If warm boot (40:e9 bit 7), skip to 1E.
1B	Set int 0F to spurious interrupt vector, check for spurious interrupts.

Code	Meaning
1C	Set int 08 (timer 0) to timer 0 int vector, enable timer and int, wait for int from timer.
1D	Timer interrupt did not occur. Init video, display error message and halt.
1E	Initialize interrupt vectors.
1F	Initialize interrupt vectors 00-6F to temporary interrupt service routine.
20	Set vectors for interrupt 02-1F.
21	Set interrupt vectors for 70-77, clear vectors 60-67 and 78-FF.
22	Clear interrupt vectors for 41 and 46 (disk parameter pointers).
23	Read 8042 self-test result from DMA page reg ch 2 (port 81).
24	Test for proper 8042 self-test result (55).
25	8042 self-test failed. Get keyboard controller status, init video, display error msg, and halt.
26	Initialize 8042 keyboard controller, transfer 128K mem. exp. bit from 8042 to CMOS RAM (IBM compatible, but not used), read state of security switch and initialize RAM variable.
27	Check Shutdown Flag = 123x. No= cold boot.
28	If cold boot or CMOS RAM is bad, install video ROM and establish video, initialize equipment flags according to primary video adapter and CMOS RAM content, initialize POST status, initialize video.
29	If not cold boot and CMOS RAM is OK, install Video ROM and establish video for mono/CGA, initialize equipment flags according to primary video adapter and CMOS RAM contents, initialize video warm boot, initialize video.
2A	Check for bad CMOS RAM and queue the message if so; command port 61 to clear parity latches, disable the speaker and disable timer channel 2; enable NMI.
2B	Check Shutdown Flag = 123x. if warm boot, use memory sizes from CMOS RAM.
2C	If cold boot, turn caches off, test memory for appropriate size, and restore cache status.
2D	Turn off POST Fail CMOS RAM bit and display any queued error messages; initialize keyboard RAM (40:17-30) + (40:E0-E7).
2E	Initialize 8042 keyboard controller and test keyboard.
2F	Initialize time of day in the real time clock chip.
30	Test for and install floppy controller.
31	Enable C&T 82C601 chip IDE interface, test for and install hard drive.
32	Test 8259 DMA registers with 55 then AA, and initialize them to 0 (ports D2 and D4).
33	Test for and initialize math coprocessor chip
34	Test for and initialize parallel and serial ports, on and off board.
35	Initialize RAM variables for bad CMOS time, date, checksum, and battery condition.
36	Wait for user to press Esc, space. Check keyboard lock, clear the keyboard lock override, beep to indicate speed, display any queued messages. Esc=setup, space=boot menu.
37	Enable system clock tick (IRQ0), keyboard (IRQ1), and slave interrupt controller (IRQ2)
38	Initialize RAM variables for Ctrl-Alt-Esc, Ctrl-Alt-Ins
39	Enter setup if user pressed Ctrl-Alt-Esc. If EISA, revert to ISA if tab key pressed.
3A	Clear screen and update equipment flags according to CMOS contents (may have changed during setup). Shadow any ROMs per setup. Enable/disable cache per CMOS RAM.
3B	Initialize floppy and fixed disk drives.
3C	Set POST Fail bit in CMOS RAM, then scan for and invoke adapter option ROMs.
3D	Clear the Shutdown Flag to 0, turn off gate A20 to enable memory wrap in real mode.
3E	Set vectors for interrupts 3B-3F, clear Post Fail bit in CMOS RAM, home the cursor, display any error messages, clear MSW of 32-bit registers (ISC Unix).
3F	Invoke INT 19 to boot operating system.

TANDY

Uses OEM version of Phoenix BIOS.

WYSE

Uses OEM version of Phoenix BIOS.

ZENITH

LEDs on system board indicate status of various stages of boot-up. All will light up first, then go out in sequence when the test is completed. May also use an AMI (Plus, normally) or a Phoenix BIOS.

Post Procedures

Procedure	Meaning
CPU	Perform read/write test on internal register. Check for defective CPU or clock generator.
ROM BIOS	Check ROM CRC value against computed value of this test. Check BIOS & I/O circuitry.
RAM	Check first 64K of memory to see if data can be stored in it so the BIOS can use it later.
DMA	Test the register functions of the DMA chips.
PIT/PIC	Perform tests on main support chips and enable appropriate interrupts. Check AC ripple.
RTC/CMOS	Check the validity of the CMOS RAM and compare value in CMOS with appropriate devices. BIOS will use the values from the CMOS to set up appropriate IRQ routines for disk and other I/O access. Check for defective CMOS/battery/adapter or CMOS setting.
Video Display	Attempts will be made to initialise video to a mono screen early on so error messages can be displayed. This test is for initialising upper video modes available with EGA/VGA.
Test/Boot to Diskette	Check floppy subsystem and prepare drive for boot if there is a bootable floppy in A:.
Boot to Fixed Disk	Initialise any fixed disks in the CMOS and give control to the first one if a bootable floppy has not been detected previously. Check for corrupt boot code if not a hardware error.

POST Codes

Code	Meaning	Code	Meaning
01	VGA check	1D	Testing system board
02	MDA initialise	1E	Testing system board
03	Initialise video	1F	Bus sizing
05	Set hard reset	20	Set BIOS data area
07	Check ROM at E000	21	Testing DMA
08	Check ROM shadow at F000	22	Checking C800 for ROM
09	Remap video to E000	24	Testing base memory
0B	Keyboard controller test	25	8042 test
0C	CMOS/8042 test	26	8042 test
0D	DMA test	27	8042 test
0E	DMA page register	28	Memory parity test

Code	Meaning	Code	Meaning
0F	Test 64K memory	29	PIT test
10	Test base memory	2A	Testing floppy disk
11	Second VGA unit	2B	Testing FDC/drives
12	Mono initialisation	2C	Testing HDC/drives
13	RTC/CMOS test	2D	Checking CMOS settings
15	CPU register test	2E	Soft configuration
16	CPU add test	30	Checking adapter ROM
17	RTC/8042 test	31	Checking CMOS settings
18	Enter protected mode	32	Enabling interrupts
19	Testing memory	33	Soft configuration
1A	Testing extended memory	34	Soft configuration
1B	Leaving protected mode	35	Jump to boot code
1C	Testing system board	00	Boot to OS

Orion 4.1E-1992

00h-1Fh and F0h-FFh are displayed after the indicated function is completed.

Code	Meaning
02	Cold Boot, Enter Protected Mode
03	Do Machine Specific Initialization
F0	Start of Basic HW Initialization for Boot
F1	Clear CMOS Pre-Slush Status Location
F2	Starting CLIO Initialization
F3	Initialize SYSCFG Register
F4	DXPI Initialization for Boot Block
F5	Turning OFF Cache
F6	Configure CPU Socket Pins
F7	Checking for 387SX
F8	82C206 DEFAULT Initialization
F9	Superior Default Initialization
FF	End of Machine-specific Boot Block
04	Check Flash Checksum
05	Flash OK, jump into Flash (FFFD Flash Code
06	Reset or Power-Up
07	CLIO Default init command
08	SYSCFG REG initialised
09	CMOS Pre-slush error words initialisation
10	SCP initialised
11	DRAM autosizing complete
12	Parity check enabled. Enable Memory Parity (EMP) LED turned off
13	Start of slushware test
14	Slushware at 000F0000h OK
15	BIOS ROM copied to slushware
16	Back in Real Mode
17	ROM BIOS Slushing is finished. CPU LED Turned off
18	Video ROM (C0000 Slushware Test
19	Internal Video ROM Slushed
1A	Back in Real Mode

Code	Meaning
1B	Internal video hardware enabled.
1C	CPU clock frequency determined
1E	BIOS RAM cleared

20-EF displayed before function has been attempted. 20-2A indicate restart after shutdown, usually return to real mode from protected mode. CMOS RAM shutdown byte (0F) has value indicating reason.

Code	Meaning
20	RESET (CMOS 0)
21	Continue after Setting Memory Size (CMOS 0F=1)
22	Continue after Memory Test (CMOS 0F=2)
23	Continue after Memory Error (CMOS 0F=3)
24	Continue with Boot Loader Request (CMOS 0F=4)
25	Jump to execute User Code (flush) (CMOS 0F=5)
26	Continue after Protected Mode Test Passed (CMOS 0F=6)
27	Continue after Protected Mode Test Failed (CMOS 0F=7)
28	Continue after Extended Protected Mode Test (CMOS 0F=8)
29	Continue after Block Move (CMOS 0F=9)
2A	Jump to execute User Code (CMOS 0F=A)
2B	Reserved
2C	Reserved
2D	Reserved
2E	Reserved
2F	Reserved
30	Exit from Protected Mode
31	TEST-RESET passed (80386). Warm Boot
32	Check the ROM Checksum. ROM LED Turned Off
33	Clear the Video Screen On
34	Check System DRAM Config Update CMOS-TOTAL-MEM-SIZE Value
35	Pro-load CMOS if CMOS is
36	Turn Off the UMB RAM
37	Turn Parity Generation
38	Initialize System Variable
39	Check for errors in POWER
3A	Initialize SCP MODE
3B	Test CMOS Diag. Power Reset
3C	Test CPU Reset 80386 & Determine State Number
3D	Save CPU ID & Processor-T
3E	Init the Video & Timers
3F	Init DMA Ports, Clear Page
40	Set Speed too Fast for Now
41	Test EEPROM Checksum
42	Enable/Disable Superior's Parallel, FDC & HDC Per CMOS
43	Slush External Video BIOS if on CMOS
44	Turn Cache off for Memory
45	Test Extended RAM (1-16Mb)
46	Test BASE RAM (0-64 OK). RAM LED turned off by Base RAM Test
47	Determine Amount of System

Code	Meaning
48	Set WARM-BOOT Flag if RES Indicates Cold Boot
49	Clear 16K of Base RAM
4A	Install BIOS Interrupt Vector
4B	Test System Timer. INT LED turned off if CLOCK Test passes
4C	(Re)Initialize Interrupt
4D	Enable Default Hardware Initialization
4E	Determine Global I/O Configuration
4F	Initialize Video
50	Init WD90C30 Scratchpad
51	Check for Errors before Boot
52	Reserved
53	Test (Ext Only) and Initialize
54	Reserved
55	Initialize the Keyboard Processor
56	Initialize the PS/2 Mouse
57	Configure CLIO for Mouse
58	Configure CLIO for LAN
59	Configure CLIO for SCSI
5A	Configure CLIO for WAM
5B	Wait for User to Enter Code
5C	Init System Clock TOD, Enable
5D	Test, Init Floppy Drive Sensor. Disk LED Turned off
5E	Check for Z150 Style Disk
5F	Init Winchester Subsystem
60	Set Default I/O Device Parameters
61	Get LAN ID Info from LAN
62	*Install ROMs at 0C8000h
63	*Install ROMs at 0E000h
64	Initialize SCSI Interface
65	Run with A2O off in PC Mode
66	Really turn off the SCP
67	Set Machine Speed using CMOS
68	Turn on Cache
69	Calibrate 1ms Constants
6A	*Enable Non-Maskable Interpreter
6B	Reserved
6C	Clear the warm-boot flag
6D	Check for Errors before Boot
6E	Boot

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Code	Meaning	Code	Meaning
0	Start of Slush Test	34	Initialize System Variables
1	Processor Test	35	Init Interrupt Controllers
2	CACHE and CLIO	36	Check Error that Occurred
3	ISP Defaults Set	37	Reinitialize SCP Warm Boot
4	Into Protected Mode	38	Test CMOS Diag, Power, Reset
5	Memory SIMMs Count	39	Reserved, or DDNIL status flag check
6	Memory Controller	3A	Test CPU Reset (80386)
7	Preped to Test Block	3B	Save the CPU ID in GS
8	First 1Mb of Ram	3C	Slush Video ROM to C0000
9	Checksum OEM ROM	3D	Init the Video and Timers
10	Low Flash ROM Checks	3E	Init CMA Ports, Clear Page
11	F000 ROM Checks	3F	Set Speed too Fast for now
12	Aurora VIDEO ROM	40	Checksum the Nonvolatile RAM
13	F000 ROM Slushed	41	Initialize Configuration
14	Sep Initialized	42	Init Expansion Boards from VRAM
15	Language Slushed	43	Turn Cache off for Memory Test
16	Do VIDEO Specific tests	44	Init Memory Ctrlr, test Extd Memory
17	Done Slushing	45	Test Base RAM
32	Point Interrupt Vectors	46	Determine amount of System RAM
33	Turn on Parity Generation		